THE INSTITUTE FOR

INTERCONNECTING

AND PACKAGING

ELECTRONIC CIRCUITS

IPC-D-317A

Design Guidelines for Electronic Packaging Utilizing High-Speed Techniques

IPC-D-317A

January 1995

A standard developed by the Institute for Interconnecting and Packaging Electronic Circuits

2215 Sanders Road
Northbrook, Illinois
60062-6135

Tel 847 509.9700
Fax 847 509.9798
URL: www.ipc.org

The Principles of Standardization

In May 1995 the IPC's Technical Activities Executive Committee adopted Principles of Standardization as a guiding principle of IPC's standardization efforts.

Standards Should:

- Show relationship to DFM & DFE
- Minimize time to market
- Contain simple (simplified) language
- Just include spec information
- Focus on end product performance
- Include a feed back system on use and problems for future improvement

Standards Should Not:

- Inhibit innovation
- Increase time-to-market
- Keep people out
- Increase cycle time
- Tell you how to make something
- Contain anything that cannot be defended with data

Notice

IPC Standards and Publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for his particular need. Existence of such Standards and Publications shall not in any respect preclude any member or nonmember of IPC from manufacturing or selling products not conforming to such Standards and Publication, nor shall the existence of such Standards and Publications preclude their voluntary use by those other than IPC members, whether the standard is to be used either domestically or internationally.

Recommended Standards and Publications are adopted by IPC without regard to whether their adoption may involve patents on articles, materials, or processes. By such action, IPC does not assume any liability to any patent owner, nor do they assume any obligation whatever to parties adopting the Recommended Standard or Publication. Users are also wholly responsible for protecting themselves against all claims of liabilities for patent infringement.

The material in this standard was developed by the IPC-D-317 Task Group (D-21a) of the High Speed/High Frequency Committee (D-20) of the Institute for Interconnecting and Packaging Electronic Circuits.

THE INSTITUTE FOR

INTERCONNECTING

AND PACKAGING

ELECTRONIC CIRCUITS

IPC-D-317A

Design Guidelines for Electronic Packaging Utilizing High-Speed Techniques

Developed by the IPC-D-317 Task Group (D-21a) of the High Speed/ High Frequency Committee (D-20) of the Institute for Interconnecting and Packaging Electronic Circuits

Why is there a charge for this standard?

Your purchase of this document contributes to the ongoing development of new and updated industry standards. Standards allow manufacturers, customers, and suppliers to understand one another better. Standards allow manufacturers greater efficiencies when they can set up their processes to meet industry standards, allowing them to offer their customers lower costs.

IPC spends hundreds of thousands of dollars annually to support IPC's volunteers in the standards development process. There are many rounds of drafts sent out for review and the committees spend hundreds of hours in review and development. IPC's staff attends and participates in committee activities, typesets and circulates document drafts, and follows all necessary procedures to qualify for ANSI approval.

IPC's membership dues have been kept low in order to allow as many companies as possible to participate. Therefore, the standards revenue is necessary to complement dues revenue. The price schedule offers a 50% discount to IPC members. If your company buys IPC standards, why not take advantage of this and the many other benefits of IPC membership as well? For more information on membership in IPC, please visit www.ipc.org or call 847/790-5372.

Thank you for your continued support.

Users of this standard are encouraged to participate in the development of future revisions.

IPC
2215 Sanders Road
Northbrook, Illinois
60062-6135
Tel 847 509.9700
Fax 847 509.9798

Acknowledgment

Any Standard involving a complex technology draws material from a vast number of sources. While the principal members of the IPC-D-317 Task Group of the High Speed/High Frequency Committee are shown below, it is not possible to include all of those who assisted in the evolution of this Standard. To each of them, the members of the IPC extend their gratitude.

High Speed/High Frequency Committee

Chairman
John Kelly
Motorola

IPC-D-317 Task Group

Chairman
Dana Korf
Zycon Corp.

Technical Liaison of the IPC Board of Directors

Rob Scott
Phase II

High Speed/High Frequency Design Subcommittee

Anton, Ronald, Honeywell Inc.
Barrett, Frank, Pacific Testing Laboratories
Bresnan, Thomas, Hadco Corp.
Buck, Thomas, Advanced Interconnection Tchnlgy
Canarr, Leslie, Rockwell International
Ecker, Bernard, Teledyne Systems Company
Ferrari, Gary, Tech Circuits Inc.
Frankosky, John, Arlon Inc.
Gibson, Joseph, Hitachi Chemical Electro-Product
Korf, Dana, Zycon Corporation
Kunkle, Robert, I-CON Industries Inc.
May, Daniel, Buckbee-Mears / St. Paul
Seymour, Suzanne, Taconic Plastics Ltd.
Sherali, Nusrat, IBM Corp./Endicott Elec. Pkgng.
Slanina, Joseph, AlliedSignal Aerospace
Thorson, Max, Compaq Computer Corporation
Traut, G. Robert, Rogers Corporation
Young, Richard, Rockwell International

Table of Contents

Figures

Tables

Design Guidelines for Electronic Packaging Utilizing High-Speed Techniques

1.0 General

1.1 Purpose The object of this document is to provide guidelines for the design of high speed circuitry. The subjects presented here represent the major factors that may influence a high speed design. This guide is intended to be used by circuit designers, packaging engineers, circuit board fabricators, and procurement personnel so that all may have a common understanding of each area.

1.2 Scope The goal in electronic packaging is to transfer a signal from one device to one or more other devices, through a conductor. Considerations include electrical noise, electromagnetic interference, signal propagation time, thermomechanical environmental protection, and heat dissipation. High-speed designs are defined as designs in which the interconnecting properties effect circuit function and require consideration. Every electrical concept has relevant physical implementation data provided to match the electrical and mechanical relationships. This guideline presents first order approximations for each of the subject areas covered. If more detail is required, the papers presented in the bibliography may provide more accurate data.

1.3 Symbology, Terms and Definitions

1.3.1 Symbology

Symbol	Description
AC	Alternating Current
CMOS	Complimentary Metal Oxide Semiconductor
COB	Chip-On-Board
CTE	Coefficient of Thermal Expansion
CTE_{XY}	X and Y-Axis Coefficient of Thermal Expansion
CTE_Z	Z-Axis Coefficient of thermal expansion
DC	Direct Current
DIP	Dual In-line Package
DWB	Discrete Wiring Board
ECL	Emitter Coupled Logic
EMI	Electromagnetic Interference
FR-4	Epoxy Glass Dielectric Material
H_L	High-to-Low Signal Edge Transition
IC	Integrated Circuit
K_B	Backward Crosstalk
K_F	Forward Crosstalk
L_G	Ground Plane Inductance
L_H	Low-High Signal Edge Transition
L_P	Power Plane Inductance
PWB	Printed Wiring Board
R_C	Series Lead Resistance
R_G	Ground Plane Resistance
R_P	Power Plane Resistance
R_T	Sheet Resistance
SM	Surface Mount
TAB	Tape Automated Bonding
Tan (δ)	Dissipation Factor (Loss Tangent)
TDR	Time Domain Reflectometer
T_P	Total Signal Line Propagation Delay Time
T_{PD}	Propagation Delay Per Unit Length
T_R	10%–90% Edge Transition Time (Rise or Fall)
TTL	Transistor Transistor Logic
Z_O	Characteristic Line Impedance (Unloaded)
Z_O'	Characteristic Line Impedance (Loaded)
ε_r	Relative Permittivity
ε_r'	Effective Relative Permittivity
δ	Skin Depth

1.3.2 Terms and Definitions The terms listed below are used in this document. Their definitions are given in order to help the new reader. These definitions are also found in IPC-T-50, ''Terms and Definitions for Interconnecting and Packaging Electronic Circuits.'' Where possible, definitions that appear in the body of this document are referred to as follows: ''Bus – 5.6.5.2''. This indicates that a definition for ''Bus'' appears in section 5.6.5.2, and will not be repeated here.

***AC Impedance*—**The combination of resistance, capacitive, reactance, and inductive reactance seen by AC and/or time-varying voltage.

***Alternating Current (AC)*—**A current that varies with time. This label is commonly applied to a power source that switches polarity many times per second, such as the power supplied by utilities. May take a sinusoidal shape, but could be a square or triangular wave shape.

***Amplitude*—**The height or magnitude of a voltage signal as measured with respect to a reference plane, such as signal ground.

***Dual-Strip Line*—**A stripline signal conductor that is embedded between two ground planes, and is not centered between them (closer to one ground plane than the other).

***Attenuation*—**Reduction in the amplitude of a signal due to losses in the media through which it is transmitted.

***Backporching*—**A term used to describe the reflections which follow a fast rise or fall time signal traveling down a long transmission line that has not been properly terminated. Looks like a stair step.

***Backward Crosstalk*—**Noise induced into a quiet line placed next to an active line as seen at the end of the quiet line close to the signal source.

***Bus*—**See section 5.6.5.2.

Busbar—A large copper or brass bar used to carry high power supply currents onto a printed board or backplane.

Capacitance—A measure of the ability of two adjacent conductors separated by an insulator to hold a charge when a voltage is impressed between them. Measured in Farads.

Characteristic Impedance—The resistance of a parallel conductor structure to the flow of AC current. Usually applied to transmission lines in printed boards and cables carrying high speed signals. Normally a constant value over a wide range of frequencies.

Circuit Board—For the purposes of this specification the term circuit board covers both printed circuit board, and discrete wiring boards where a circuit function is performed.

Coaxial—A term used to describe conductors that are concentric about a central axis. Take the form of a central wire surrounded by a conductor tube that serves as a shield and ground. May have a dielectric other than air between the conductors.

Crossover—Intersection of two conductors separated by insulation.

Crosstalk—See section C 3.2.

Current—Electrons traveling in a conductor as the result of a voltage difference between its ends.

Decoupling—Absorbing noise pulses generated in the power supply lines by switching logic so as to prevent them from disturbing other logic on the same power supply circuit. Usually done with capacitors. See 5.1.3.

Differential Pair—Parallel routed signals exhibiting a mutual impedance between both lines, typically 50 to 120 ohms.

Direct Current (DC)—A current produced by a voltage source that does not vary with time. Normally provided by power supplies to power electronic circuits.

Discrete Wiring Board—Circuit board using round insulated wire to form signal paths, terminated by a plated through hole.

Dissipation Factor—A factor used to express the tendency of insulators or dielectrics to absorb some of the energy in an AC signal.

Edge Rate—The rate of change in voltage with time of a logic signal transition. Usually expressed in volts per nanosecond.

Edge Transition Attenuation—The loss in sharpness of a switching edge caused by absorption of the highest frequency components by the transmission line.

Effective Permittivity (Dielectric Constant)—See section 5.2.2.

Effective Relative Permittivity—See section 5.2.2.

Electromagnetic Interference (EMI)—Radiated electromagnetic energy which couples into conductors where it is not wanted.

Flat Conductor—A rectangular conductor that is wider than it is high. Usually refers to signal conductors in a printed wiring board.

Forward Crosstalk—Noise induced into a quiet line placed next to an active line as seen at the end of the quiet line farthest from the signal source.

Ground—A term used to describe the terminal of a voltage source that serves as a measurement reference for all voltages in the system. Often the negative terminal of the power source, but sometimes the positive terminal.

Impedance—The resistance to the flow of current represented by an electrical network. May be resistive or reactive, or both.

Inductance—The property of a conductor that allows it to store energy in a magnetic field induced by a current flowing through it. Units of measure: Henry.

Line Coupling—Coupling between two transmission lines caused by their mutual inductance and the capacitance between them.

Load Capacitance—The capacitance seen by the output of a logic circuit or other signal source. Usually the sum of distributed line capacitance and input capacitances of the load circuits.

Logic—A general term used to describe the functional circuits used in computers and other digital electronics to perform computational functions. Logic Family—A collection of logic functions or ICs using the same form of electronic circuit to perform computation. Examples: ECL—emitter coupled logic; TTL—transistor-transistor logic; CMOS—complimentary metal oxide semiconductor logic.

Microstrip—See section 5.5.1.

Net—See section 5.6.5.1.

Parallel Pair—Two conductors that travel side by side at a controlled spacing over a long distance.

Permeability—A general term used to express various relationships between magnetic induction and magnetizing force.

Permittivity (dielectric constant)—See section 5.2.

Power Dissipation—Energy used by an electronic device in the performance of its function.

Power Plane Inductance—See section 5.1.2.1.

Printed Wiring Board—A circuit board utilizing etched copper traces for signal interconnections.

Propagation Delay—The time required for a signal to travel along a transmission line, or the time required for a logic device to perform its function and present a signal at its output.

Pulse—A logic signal that switches from one state to the other and back in a short period of time, and remains in the

original state most of the time. Usually used as clocks for logic devices.

Reflection—Energy from a high speed signal edge that is sent back toward the source as a result of encountering a change in impedance in the transmission line on which it is traveling.

Rise Time—Time required for a logic signal to switch from its low state to its high state. Commonly measured between the 10% and 90% voltage levels.

Signal Line—Any conductor used to transmit a logic signal from one circuit to another.

Skin Effect—See section 5.8.1.

Stripline—See section 5.5.3.

Stub—A branch of the main line of a signal net usually used to reach a load that is not on the direct signal path.

Transmission Line—Any form of conductor used to carry a signal from a source to a load. The transmission time is usually long compared to the speed or rise time of the signals, so that coupling, impedance, and terminators are important to preserving signal integrity.

Waveguide—A rectangular or round tube used to transmit microwave energy in the form of an electromagnetic wave rather than a current in a wire.

1.4 Units Unless otherwise specified, dimensions will be metric (SI).

2.0 Applicable Documents

IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits

IPC-L-125 Specification for Plastic Substrates, Clad or Unclad for High Speed/Frequency Interconnections

IPC-MF-150 Metal Foil for Printed Wiring Applications

IPC-D-275 Printed Board Design Standard

IPC-D-249 Design Standard for 1 and 2 Sided Flexible Printed Boards

IPC-DW-424 General Specification For Encapsulated Discrete Wire Interconnections Boards

IPC-DW-425 Design End Product Requirements for Discrete Wiring Boards

3.0 Overview Packaging of electronic equipment has traditionally been an area for mechanical considerations. An assortment of active and passive devices need to be adequately provided with physical support, environmental protection, heat removal, electrical interconnections where specified and electrical insulation where interconnections are not specified, all by a cost-effective means.

Packaging design is becoming more complex. Switching devices typical of digital electronics technology are available in increasingly greater degrees of both switching speed and count of devices per chip. Individual chips are being provided with greater numbers of connections in smaller individual chip package sizes. The competitive need to take maximum advantage of device density and speed has forced packaging designers to pay much more attention to problems of electromagnetic wave-propagation phenomena associated with transmission of switching signals within the system. New design disciplines and design strategies are needed. This document is intended to help meet this need and this overview section will introduce in broad terms what is covered.

3.1 Decision Making Process Determine at the start of a project whether packaging concerns need early introduction into the design process. Performance of older systems was limited by the devices available and packaging design could be left for the end of the design activity. High performance systems are limited in speed by packaging, so if the project is concerned with speed, start by considering how to get the most out of the packaging.

There are numerous design options to consider, balanced against mechanical and electrical requirements of the package (see Figure 1). For a proposed system, a choice among types of devices has to be made. This will have an influence on the kinds of packaging materials to be selected. It will become apparent that the design is a collection of compromises to get the best overall performance. Effort early in a program to evaluate many sets of options and their interactions is recommended.

The decision making cycle will consist of proposing a design with selection of devices, packaging materials, and interconnection scheme. The system preferably will be modeled and its deficiencies and limitations identified. This should result in some alterations in the design as the start of another modeling cycle. The process is repeated until further improvement is minimal. If the projected performance is far short of the target then the designer should consider attempting a different design approach.

These guidelines should be helpful in providing awareness of the options available and the principles needed in modeling. There is plenty of room for innovative advances in high speed packaging.

3.2 Design Options Let us consider some of the options to be exercised by the designer, realizing that each selection interacts with the others. These are organized as options that may be considered as givens followed by a list of the resulting requirements.

3.2.1 System Electrical/Mechanical Givens What type of active switching devices will be used? Example options include TTL, Schottky TTL, CMOS, ECL and GaAs, each with its own set of power requirements, operating temperature range, density on a chip, input impedance, output impedance,

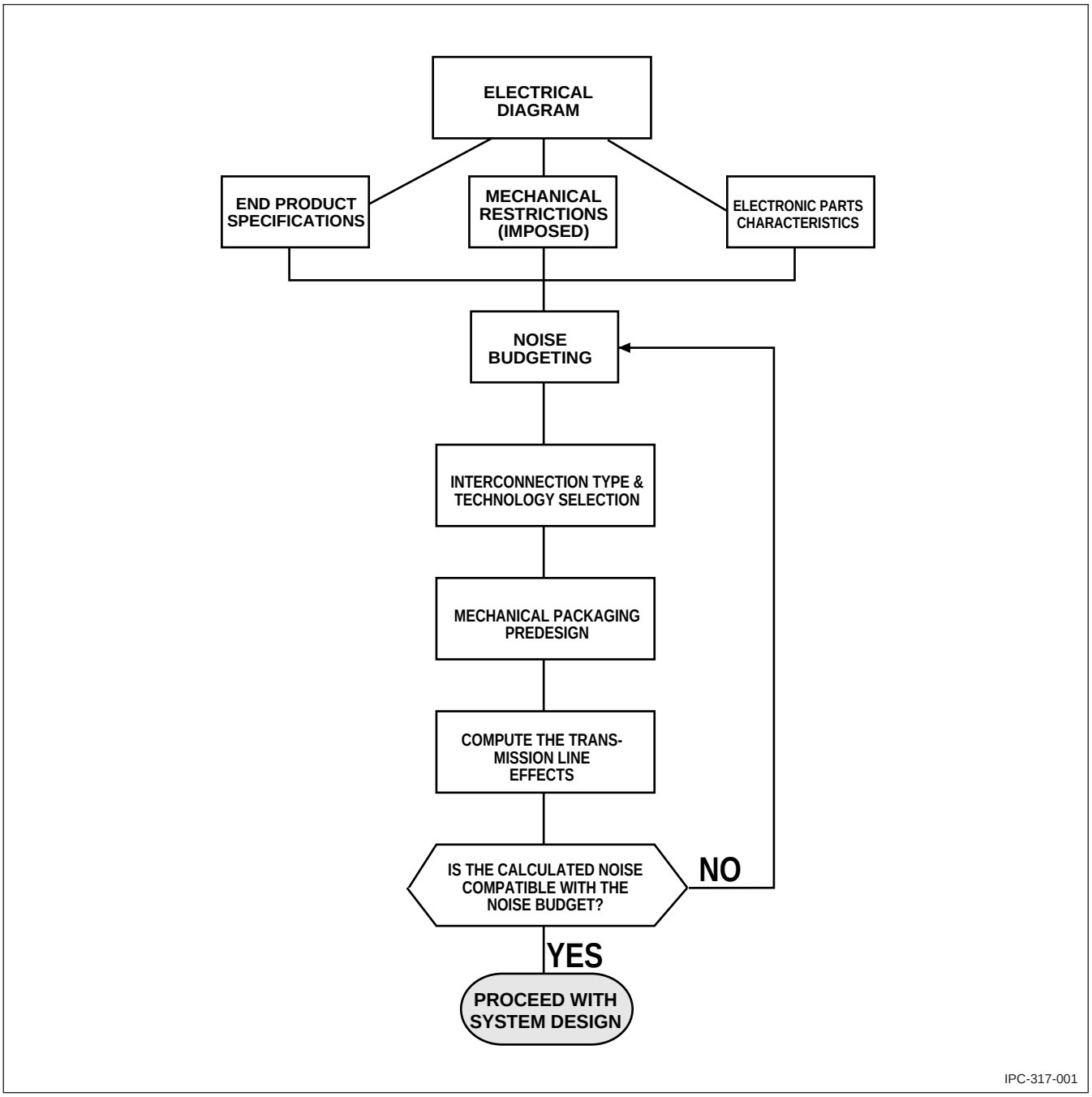


Figure 1 High speed packaging design concept

signal threshold levels, noise sensitivity, response time and output pulse rise/fall time.

How will devices be organized in the final assembly? Chip devices can be prepackaged and individually mounted on a large board or assembled into small boards or multichip modules which will in turn be mounted onto large boards. Large systems will require several large board assemblies and there is yet another option of how this level of interconnection will be applied. Reflection noise and signal degradation will accompany transitions from one packaging level to the next. Organization will have an impact on manufacturability and repairability of the system.

What transmission line geometry on boards will be used for signal interconnections between devices? Options include coplanar coupled pairs, microstrip over a single ground plane, striplines between ground planes, orthogonal striplines sharing a common pair of ground planes, wire over ground plane, and wire between ground plane. For a given geometry the selection of substrate thickness and conductor width will depend on the required characteristic impedance, the relative permittivity (dielectric constant) of the substrate and its thickness.

What interconnect schemes for signal transmission will be used? One could choose single connections from one device

output to another device input. A single output could be connected to several inputs and the multiple connections could be accomplished either by branching or by continuing from one input to the next in daisy-chain fashion. The scheme will affect transmission time, noise, settling time and signal pulse degradation.

3.2.2 System Electrical/Mechanical Requirements The decision on the number of signal layers in multilayer boards or discrete wiring boards will be influenced by the density of interconnections within the board. There will be a compromise of the degree of isolation of one interconnection from another versus the need to get a large number of interconnections in a given board area.

Determine the degree of crosstalk or coupling between signal lines that can be tolerated. This can have a major effect on acceptable interconnection densities.

Relative permittivity (ε_r) influences board substrate selection. While a low ε_r value means faster signal propagation it also increases the conductor width needed at a given substrate thickness for a given characteristic impedance, thus reducing room for conductors.

Power requirements of the devices will need to be met by an adequate scheme. Often the choice is made to provide voltage planes in circuit boards that serve the dual roles of ground plane for signal conductors and leveled supply of voltage to devices. An alternative is to provide a bus system to the array of chip devices on the board.

3.3 Mechanical Requirements The mechanical requirements list is derived to assure a means to maintain the integrity and performance of electrical interconnections among electronic devices in the system.

3.3.1 Circuit Board Circuit boards are required to provide mechanical support and interconnection of components mounted on them. Space constraints, number and complexity of interconnections, thermal management, power distribution and cost of manufacture are some factors to be considered when determining requirements of how many layers, the thickness of dielectric layers, the composition and thickness of ground/voltage plane layers, the dielectric composition and the overall length, width, and thickness.

3.3.2 Hybrid This term is often used to refer to assemblies of thin/thick film chip devices mounted directly on thin/thick film ceramic interconnection boards to form a multichip module. Other technologies using polymeric substrates in place of the thin/thick film ceramic could also be used to build multichip modules. Hybrid boards and multichip modules are usually required to provide protection of sensitive chip components from adverse effects of whatever ambient atmosphere may be encountered in service. They also must be able to withstand thermal and mechanical shock during manufacturing and assembly as well as in service.

3.3.3 Component Packaging Unless chip devices are packaged in multichip modules or hybrid subassemblies they are usually prepackaged individually. The component package can be polymeric or ceramic depending on the degree of atmospheric protection required. The package is required to provide protection to the chip and electrical connections from the chip to the board on which it will be mounted. The package also provides a means for connecting to the chip for automated testing of the package prior to its being used in a board assembly.

The electrical connections to the board can be of a variety of configurations ranging from pins that will insert into plated through holes provided in the board, as in dual in-line package, to a series of metallized regions along the edge or arrayed over the base of a surface mount device. What type of connection is selected will depend on, among other things, the requirements for electrical performance of the connections.

Requirements for component packaging will be dependent on many factors including space available, economics, electrical performance requirements, reliability, life expectancy, and thermal conditions.

3.3.4 Thermal Management The system must withstand thermal cycling and temperature differences during service. Temperature differences arise, especially in startup, between packages containing chips and the supporting interconnecting boards that will generate strains due to thermal expansion. Use of materials with differing coefficient of thermal expansion (CTE) in different levels of packaging will lead to strain between these levels as temperature changes on the connections.

The packaging materials must handle the heat generated by operating the system. Mechanical properties sufficient to provide mechanical integrity of the system must be retained at the elevated temperature expected to be encountered during system operation. Packaging must provide for removal of excess heat to keep the temperature below the point where impairment of electronic performance would occur.

3.3.5 Component Mounting The component must be provided in a format that is convenient to attach to the circuit board. Mechanical requirements imposed on the board include tolerances of size and location of the features involved in the attachment and ability of it to withstand thermal shock and stress involved in the attachment of the component. Some device packaging categories include:

a. COB mount device

b. TAB mount device

c. Single chip package (DIP, PLCC)

d. Multichip package

3.4 Electrical Considerations Electromagnetic wave propagation theory must be considered in evaluating the performance of interconnecting conductive conductors and their substrates. High-speed devices are characterized by the short rise time of the pulses. The pulse wave form may be represented as the sum of a series of sinusoidal component signals with certain phase and amplitude relationships. As the rise time of the pulse decreases, the frequency of the important components increases.

3.4.1 Power Distribution For high-speed devices, switching activity is accompanied by equally high-speed demands for changes in electrical current from the power supply. If several devices are demanding current changes at or near the same instant, the power distribution system is required to meet these demands while it is maintaining voltage within specified limits to all devices being supplied. Meeting this requirement demands low inductance connections to devices, with high capacitance among various voltage levels in the distribution system.

3.4.2 Permittivity The relative permittivity (ε_r) of the dielectric substrate of an interconnecting device, whether it be a printed board, discrete board and a multichip module, or a chip package will affect electrical performance of the interconnection on or embedded in it. An assumed ε_r is used in the design of the interconnection to meet the impedance, capacitance and propagation time requirements as will be discussed. The tolerances of these requirements along with manufacturing tolerances on conductor dimensions impose a tolerance requirement on ε_r if the system is to perform as designed. Since ε_r of many substrate materials varies with composition, frequency, and environmental conditions this also impacts on allowable tolerances in ε_r.

For a given transmission line geometry propagation time will vary directly as the square root of ε_r, impedance inversely as the square root of ε_r, and capacitance directly as ε_r.

There are trade-offs in the selection of high or low ε_r values for the substrate that will be discussed later.

3.4.3 Capacitive Versus Transmission Line Environment

For an interconnection from one device to another, the connecting line can either be treated as a transmission line or a capacitive line. For transmission lines the design concept is to provide a known characteristic impedance that is terminated at the destination with a matching impedance to minimize reflections resulting from fast rise time pulses. For a capacitive line, the concept is that of a line whose stored charge requires a certain amount of current flow to result in changed voltage detected at the destination. The critical design parameters and requirements will depend on which concept is appropriate.

3.4.4 Propagation Time In high-speed systems, it is not unusual for the clock cycle time to be shorter than the propagation time for a signal from one device to another, especially where a signal might originate on one board and be received on a device on another board. For the system to perform correctly at high speeds, a well controlled propagation time is required and in some cases adjustments in the propagation time for certain lines may be required.

3.4.5 Impedance The reason why 50 to 70 ohms characteristic impedance is so often used is that lower Z values cause excessive dI/dt crosstalk, and can double the wattage consumed and the heat dissipation problem. Higher impedances not only permit higher crosstalk values, but produce circuits with greater EMI sensitivity, and greater EMI radiation. There is less and less use of impedances much removed from 50 ohms. The impedance is the square root of the ratio of inductance per unit length to capacitance per unit length. The impedance of a transmission line can be mathematically modeled as a complex function of several parameters:

a. ***Conductor width/diameter***—lower impedance with wider line width or larger diameter

b. ***Type of conductor***—coplanar pair of conductors, microstrip with one ground plane or stripline between two ground planes. With equal ε_r, spacing and conductor width, impedance ranking will be coplanar > microstrip > stripline.

c. ε_r ***of dielectric***—lower impedance with higher ε_r

d. ***Spacing between signal and ground***—lower impedance for smaller spacing

e. ***Proximity to other conductors***—lower impedance as proximity increases

3.4.6 Signal Loading Effects When a conductor proceeds to several loads (termed ''signal line''), the issue of signal loading must be considered.

Consider loads connected in daisy chain fashion. If the impedance of the load is low or a near match to the characteristic impedance of the line there will be a decrease in signal amplitude as each load is reached. High-impedance loads relative to the line will result in less decrease in amplitude. A matched load at the end load is needed to prevent a reflection that could send a false pulse to the other points. The transmission line concept is usually appropriate.

With a star connection scheme, each branch point looks like a low impedance load and the amplitude will be diminished on the branches. The capacitive line concept is usually appropriate.

3.4.7 Crosstalk In general, an interconnecting board is populated as densely as possible with chip devices to minimize the size of the system and reduce propagation time. The result is that conductors must be run close to each other and usually the designer must resort to multilayer boards or discrete wiring boards to handle the high interconnect density and the crossover situations in the wiring plan.

Cross talk is the transfer of pulse energy by the electromagnetic field from a source line to a victim line. The intensity of the transferred (coupled) signal decreases with shorter adjacent line segments, wider line separations, lower line impedance, and longer pulse risetimes.

A victim line could run parallel for short distances to several other lines. If a certain combination and timing of pulses on the other lines occurs, it could induce a spurious signal on the victim line. Thus, there are requirements that the crosstalk between lines be kept below some level that could cause a malfunction of the system.

3.4.8 Signal Attenuation High-speed systems have devices that generate short rise time pulses and may respond ambiguously to pulses exceeding a certain maximum rise time. Signal attenuation increases rise time and decreases the amplitude of the pulse. This is best explained in terms of the model of a pulse as a sum of signals of several frequencies. The high frequency components of the pulse attenuate more rapidly than lower frequency components. This is due to the skin effect in the conductor as well as the dissipation effect in the dielectric.

For thin copper, the pre-treatment may raise the copper impedance.

Signals may be further attenuated by the resistance of the copper used in the conductor and by skin effect losses resulting from the finish of the copper surface.

The resistance of the copper may reduce the steady state voltage levels below the levels needed for adequate noise immunity. This is especially true of ECL circuits where a voltage divider is formed by the terminating resistor and the line resistance.

DC resistance can be calculated using the copper resistivity and the geometries of the conductors being used. The effects of surface finish (skin effects) may have to be determined by experiment. The smooth surface of a drawn wire used in discrete wiring boards has lower skin effect losses and other advantages over etched conductors.

4.0 Mechanical Considerations In addition to meeting the predicted performance criteria, circuit board designs must be manufacturable if the system is ever to become a reality. Performance versus cost also factors into the choice of the optimum system design. Yield at manufacture and end product reliability may be, at times, even greater contributors to cost than the obvious costs of raw materials and fabrication. For this reason, the designer should be familiar with the material options available, their properties, capabilities, and tolerances and have a reasonably good understanding of process capabilities and tolerances that may impact, not only performance but also manufacturing yield and reliability.

The development of a close working relationship with the manufacturing engineering group of the captive or vendor board fabrication facility is highly useful to avoid excessive prototype iterations which are both costly, and time consuming. Designing ''based on what worked before'' is certainly valid but may be limiting at times if full advantage of advances in both materials and fabrication is to be taken. Therefore, the development of a relationship with in-house advanced materials and manufacturing groups as well as outside industry sources is advisable.

The following is intended to serve as a cursory overview of some of the interactions between raw materials, performance, and manufacturing capabilities. This summary should by no means be considered exhaustive of the technologies available for the production of circuit boards.

4.1 Printed Board

4.1.1 Substrate Materials A table of generally available laminates is in Appendix B. Refer to IPC-L-125, ''Specification for Plastic Substrates, Clad or Unclad for High Speed/High Frequency Interconnections'' for more detailed information. These materials are classified by the resin system and support material or filler that make up the composite and are responsible for their individual electrical, chemical, and physical characteristics.

4.1.1.1 Resin Systems The resin systems used for circuit board laminates are classified into two basic categories: thermosetting and thermoplastic. Thermosetting resins are crosslinked matrices of smaller, polymeric units. The polar nature of materials generally contributes to higher relative permittivity, loss tangent (dissipation factor) and water absorption. The crosslinked structure of the thermosets generally provides better dimensional and thermal expansion characteristics. Water absorption becomes an issue because its relative permittivity is so high (approximately 75) compared to these resin systems. Therefore, relatively small changes in humidity in the environment may drastically impact performance (i.e., capacitance + Z_o) and necessitate strict environmental controls. Likewise, each resin system has a characteristic response of relative permittivity and loss tangent to temperature and operating frequency.

4.1.1.2 Reinforcements, Supports, and Fillers Although some of the available materials are comprised of resin only, routinely various reinforcements, supports, and/or fillers are incorporated with the various resin systems to enhance the physical or electrical properties of the composite laminate. A typical example is the incorporation of woven E-glass into a resin matrix to enhance dimensional stability and reduce the X-Y coefficient of thermal expansion (CTE_{XY}) which may be unacceptable or undesirable in the unsupported resin. Fillers may be added to modify the relative permittivity and/or to exclude resin and thereby reduce the overall CTE in X, Y, and Z dimensions.

The thicknesses of woven glass reinforced materials are typically even multiples of the reinforcement thickness plus resin.

4.1.1.3 Claddings Copper is by far the most common cladding material around which most circuit board processes have been designed. Copper foils are sold by weight, with 1/2 (153), 1 (305), and 2 (610) oz.,/ft^2 (gm/m^2) being common. These weights roughly translate to 0.7, 1.4, and 2.8 mils in thickness respectively. Thinner foils are available.

For high speed circuitry it may become necessary to provide special cladding material:
– with reduced (inner) surface roughness (≤2µm) in order to minimize line resistance
– permitting advanced interconnection techniques (e.g. ultrasonic bonding)

Copper foils are available in rolled annealed or electrodeposited forms. Other properties of copper foils relate to their ductility and elongation characteristics which may impact through-hole reliability. For more information on foils, consult IPC-MF-150, ''Metal Foil for Printed Wiring Applications.'' Untreated copper foils shall have the following maximum resistivity at 20°C.

For deposited foil:

Weight Designator

E ..... 0.181 ohm-gram/meter^2

Q ..... 0.171 ohm-gram/meter^2

T ..... 0.170 ohm-gram/meter^2

H ..... 0.166 ohm-gram/meter^2

M ..... 0.164 ohm-gram/meter^2

1 oz. and over (305 gr/m^2) ..... 0.162 ohm-gram/meter^2

For wrought foil (all weights):

Type 5, 8 ..... 0.158 ohm-gram/meter^2

Type 6 . 0.153 –0.157 ohm-gram/meter^2 according to temper

Type 7 ..... 0.152 ohm-gram/meter^2

4.1.1.4 Discrete Wiring For high-speed circuitry utilizing discrete wiring boards the following insulated wires are used:

Diameter	AWG	Resistivity @ 20°C
2.5 mil	42	1.80 ohms/ft
4.0 mil	38	0.648 ohms/ft
6.3 mil	34	0.261 ohms/ft

4.1.1.5 Prepregs, Bonding Layers and Adhesives Various thermosetting and thermoplastic materials are available for laminating the multilayer package. Prepregs are woven glass supported resins in their B-stage or partially cured state. They are used to create the dielectric spacing between layers and are cured or crosslinked in the lamination process. Thermoplastic bonding layers may also be used for dielectric spacing and work by fusion bonding in lamination cycles exceeding their melting point. Thermoplastic bonding films and thermosetting adhesive films are thin unsupported materials used in configurations where the dielectric spacing is already provided by another material.

4.1.1.6 Material Tolerances Knowing the raw material tolerances from the outset will go a long way toward predicting the probability that a given design will perform within the desired specifications and form the basis for any sensitivity analysis. Impedance calculations are heavily impacted by thickness (dielectric spacing) and relative permittivity; therefore, these are of primary interest.

1. ***Relative Permittivity (ε_r)***–The relative permittivity of the unreinforced materials should be invariant as these are generally uniform, isotropic materials. The reinforced, supported, and filled materials are combinations of materials of different relative permittivities and will exhibit variations in this value unless the proportions of the combination are strictly controlled.
2. ***Thickness***–Changes in the volume percent of resin will impact both thickness and relative permittivity. Thickness uniformity among materials will vary with the technology and the level of process control employed.

4.1.1.7 Material Impact on Board Fabrication/Assembly

The specific details of circuit board manufacture are not discussed here. However, the effect of materials properties on manufacturing issues are listed as they impact design considerations. This list is not exhaustive.

1. ***CTE_{XY}***—The expansion characteristics of the printed board under thermal load will impact the choice of components, the style of leads, and the method of mounting to minimize CTE mismatches which may ultimately reduce joint reliability. The reverse is also true. If the choice of component package and lead has already been made, then the material choice follows. In other cases, other materials may be incorporated into the package to further constrain movement in the X-Y plane further reducing any CTE mismatch. Various thermal management schemes may also provide some relief in this regard.
2. ***CTE_z***—Thermal expansion in the z-axis may impact through-hole (PTH) reliability in fabrication, assembly and in service. Advanced techniques or controls may be required to utilize high z-axis expansion materials. The number of layers or the overall thickness of the package may have to be limited or in some cases may preclude the use of PTH's altogether. Use of discrete wiring for replacing multiple etched signal layers can significantly reduce board thickness and eliminate z-axis expansion concerns.
3. ***Young's Modulus***—The ratio of unit stress to unit strain
4. ***Poisons Ratio***—The ratio of lateral strain to longitudinal strain
5. ***Dimensional Stability***—Dimensional changes in the material impact layer-to-layer registration. Advanced techniques or controls may be required to utilize less stable materials.

6. ***Thermal Properties T_g—***The glass transition temperature T_g of the material will dictate the thermal processes employed either in fabrication or component attachment.
7. ***Chemical and Solvent Resistance—***These properties will dictate chemistries that can and cannot be used for processing and cleaning.
8. ***Machinability—***The relative ease with which a material can be drilled, punched, and routed will impact the cost of fabrication.

4.1.1.8 Circuit Board Fabrication and Tolerances A general understanding of the capabilities of board fabrication technologies and the realistic and achievable tolerances is critical to the successful implementation of designs. Areas of particular interest are:

a. ***Hole location and diameter—***impacted by drills, material, dimensional stability, drilling practices, and plating.
b. ***Conductor width and spacing—***impacted by artwork, imaging, copper foil thickness, etching and plating. The DWB conductor is determined by wire size selection, and can be spaced on a variable XY grid or on the 45 degree diagonal.
c. ***Conductor geometry—***impacted by imaging technique, cleaning, etching and plating. The DWB inherent wire uniformity is not affected by subsequent fabrication processing.
d. ***Dielectric spacing—***impacted by choice of prepreg or bonding layer or film and lamination conditions.

Note: Prepreg thickness (and therefore permittivity) may vary with pressing conditions. For calculation purposes, the designer should consider the effective permittivity and thickness of a prepreg after the lamination cycle and account for any permittivity mismatches that may exist between the prepreg and other layers.

4.2 Component Packaging

4.2.1 Device The component package must be considered when selecting high speed design rules and determining properties. The device package will establish thermal and electrical guidelines. In passive components the predominate factor will be the lead length. The leads provide additional inductance and capacitance which will affect propagation speed and switching transients. To minimize these effects the leads should be trimmed as short as possible or removed. Surface Mount Device packaging can provide leadless devices which can be directly mounted to the interconnecting substrate. It is important to note that component data sheets often do not provide parasitic values for high speed noise and propagation speed calculations.

Active devices, such as integrated circuits, are often offered in several package styles that provide various electrical and thermal performances. In general use, DIP packages have been the predominate package in either plastic or ceramic. These typically are the largest packages and provide the worst high speed operating environment. The next best package style is the Surface Mount Package. These are offered in either Chip Carrier or Small Outline IC packages. These typically will reduce the lead capacitance and inductance. SM packages can easily be automatically assembled and handled. To obtain the optimum performance from the device, assuming operating conditions and reliability standards can be met, the die should be directly mounted to the substrate using either the Chip-on- Board (COB) or Tape Automated Bonding (TAB) approach. These offer the optimum approach since no additional capacitance or inductance is added with the exception of the bond wire (for COB) or copper conductor (for TAB).

4.2.2 Connectors Board to board connections are often the most troublesome high speed connections because a continuous signal path is not possible due to mechanical constraints. There are two primary approaches to reduce the signal discontinuity.

The first approach assumes that the connector style is fixed, so the pinout must be modified to provide a good signal path. Non-differential signals reference between the active signal line and a reference plane; either a voltage or ground plane, whichever is closest.

Board to board connections are often troublesome because of mismatches in characteristic impedance. Non-differential signal conductors rely on controlled geometries and nearby AC reference planes (either DC voltage or ground planes) for impedance control. These geometries are interrupted in the connector.

Efforts to control signal and reference pin quantity and location in the connector should be made to control electrical performance.

To reduce the noise more reference pins must be added to reduce the distance and sharing problems. Generally a 3:1 signal:reference pin ratio is sufficient. The best ratio is 1:1, but may be too expensive, or consume too much real estate.

The second approach is to modify the connector. The intent is to minimize the discontinuity distance between boards. Either shortening the pin length, or adding reference ground plane within the connector can be used.

4.2.3 Cables High-speed cables must provide a good signal environment. There are three areas that must be considered; signal propagation speed, crosstalk, and induced noise.

Crosstalk can be minimized by several methods. The easiest is to put ground lines between the signal lines to isolate adjacency. A ground plane can be added which lowers the signal line impedance. The best method is to completely isolate signals using a coax line environment. This provides total isolation, but also is the least dense approach.

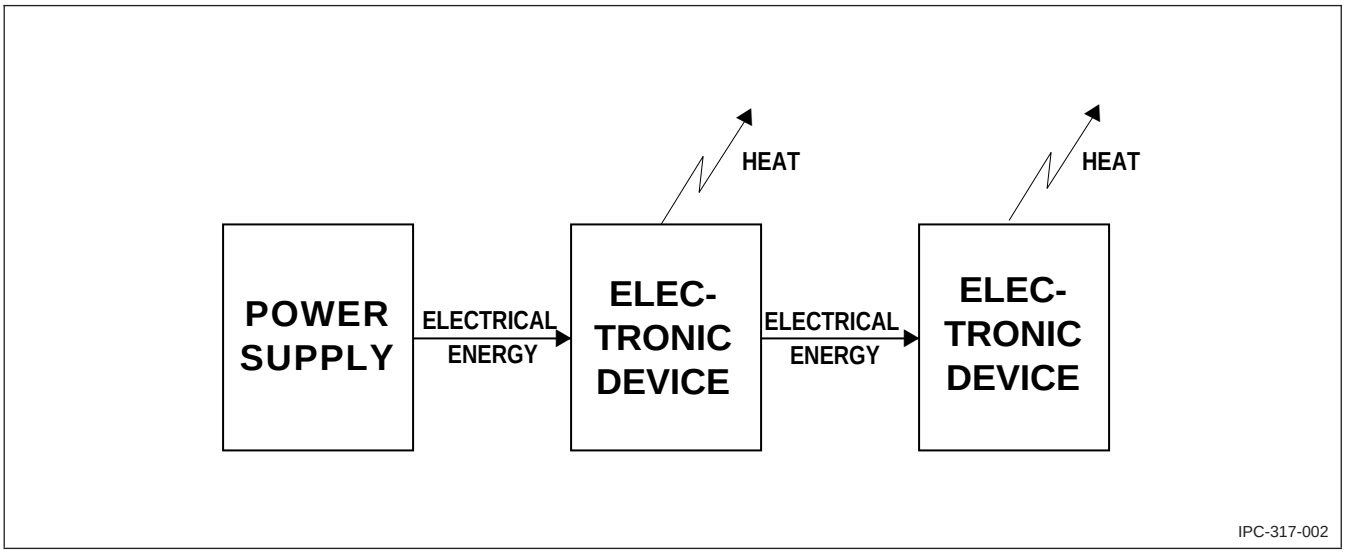


Figure 2 Schematic of information, electrical power, and enthalpy flows

Induced noise coupled onto the lines can be lowered by putting a shield between the signal line and the radiating source. This can be accomplished by using the ground planes mentioned above, or providing an additional shield plane over the entire structure.

4.3 Thermal Considerations Electronic equipment processes information at the expense of electrical energy. The electrical energy fed to the machine is converted into other forms of energy and dissipated into the machine environment. There are two main ways of dissipating this energy;

- electromagnetic radiation and
- heat (thermal energy)

The electromagnetic radiation is generated because interconnections between two points on a board act as an unintentional antenna. The greater the area enclosed by the loop and the higher the frequency and the input current, the higher the level of energy radiated from the system. Even though the continuous increase of signal speed in equipment increases the amount of radiation, the quantity of energy lost in this way is negligible when compared with the quantity of energy converted to heat. Because industry regulations limit the amount of energy radiated from the system in the form of electromagnetic waves, this form of energy is generally captured by enclosures and eventually transformed into heat before it dissipates to the environment.

In order to understand the new aspects of the problem created by increasing the signal speed, one has to start by considering that with slower technologies the partitioning of the board is independent of the electrical signal characteristics. Under such conditions, the device positioning on the board and the interconnect routing can be done keeping a few considerations in mind, such as thermal requirements. Under the high-speed conditions, the characteristics of the signal will practically dictate the positioning of the device, the routing of the interconnections, and the material to be used as well as the size and characteristics of the device package. All of these determinants will have very strong impact on the selection of the cooling option and the entire thermal design of the system.

4.3.1 System Level Impacts The increasing of the signal speed is necessary because it can increase the quantity of information that is processed per unit of time. As mentioned before, electronic equipment processes information at the expense of energy (electrical) which is absorbed from the source and lastly transformed into heat which must be removed from the system. For example, Figure 2 shows a schematic representation of flows of information, electrical energy and heat in a computer room environment.

With electronics becoming more powerful due to the use of high speed technology the energy required to operate the whole system of information processing and heat disposal is becoming a matter of great concern to both the manufacturer and customer alike. Translating this issue into thermal terminologies; ''high speed'' often means more heat dissipation per unit volume. Ambient air generally is the ultimate heat sink, therefore it is expected that the temperature of this air will increase resulting in a ''hotter'' environment for any considered device. The possible solutions at the system level are:

- increasing ventilation in order to reduce the air temperature by injection of cold air from outside
- use of heat exchangers (air to water or coolant) in order to evacuate the heat accumulated in the air in such a way as to reduce the ambient air temperature
- use of active mechanical systems for air conditioning
- replace the air as a cooling agent with other fluids which have a higher specific heat capacity and are easier to circulate and refrigerate (such as water, freons and other organic fluids)

4.3.2 Board Level Impacts The effect of heat on high-speed signals can be immense. Electronic signals typically degrade as the temperature increases. Slower signal transition times result and they may become more sensitive to system electrical transients.

The success of any approach depends mainly on the ability of the designer to find a way to ''spread'' the concentrated heat over a larger area in order to reduce the peaks of the temperature field created by uneven power dissipation. This task is especially difficult today when we consider the properties of the materials involved in high-speed technology: materials with a low permittivity are needed, but these tend to have very poor thermal conductivity as well. For example, in order to spread the heat conducted by an active device, hybrid technology with a ceramic substrate is usually utilized. If the requirements for speed are very high, ceramic substrates may not be a viable option because they have a permittivity 2 to 4 times that of FR-4 glass epoxy. Possible solutions to confine this problem are;

- better air flow management that ensures directing of the air to overheated areas
- conduction cooling and thermal spreaders (the heat is conducted to larger areas from which it can be removed)
- immersion of the electronics in dielectric fluids

Immersion cooling could be considered a very costly, efficient way of dealing with both high power dissipations as well as uneven dissipations of high concentrations in small volumes.

Beside the capability to spread heat rapidly into the entire volume of the enclosure these fluids can also act as cooling agents by absorbing the heat from the devices and transferring it either to another cooling loop or directly to the environment. The boiling temperature of the immersing fluid can be selected in such a way as to coincide with the maximum temperature admissible in the system. Phase changing of the fluid (boiling and condensation) could practically maintain the temperature of the electronics at a preset constant.

In order to understand the impact that high-speed technology has had on thermal design one has to consider the multi-chip modules symbolized in Figure 3 by double circles. High speed multi-chip modules are created by joining together a certain number of semiconductor chips with controlled impedance transmission lines in order to achieve particular electrical performance. However, grouping the devices close together in order to reduce interconnection distance may produce localized hot spots.

4.3.3 Device Level Impacts The component package has a direct impact on the performance of the device. At the same time the thermal characteristics of the device package are worsening almost linearly with the decrease of the device size. Generally, a way of improving the device package thermal performance is the use of ceramic materials for enclosures. As specified in the previous discussion ceramic materials have higher electrical permittivity which will negatively impact electrical performance of the package if very high-speed devices are involved. Low permittivity materials that improve the electrical performance tend to be very poor thermal conductors and also trap heat inside the semiconductor enclosure. Higher speed is usually associated with a temperature rise in the semiconductor itself and thus presents an important challenge when high reliability of the product is required. Reliability decreases as temperature rises.

4.4 Component Placement Component placement is a critical factor in the design of high-speed systems. The effects of improper placement can be significant and include concerns in the following areas.

– Crosstalk Management

– Impedance Control

– Power Distribution

– Thermal Management

– System Cost

4.4.1 Crosstalk Management Typically, crosstalk is a concern when high-speed devices are used because of the high harmonic frequency content. Mixing logic families also causes concern because of the mixture of various voltage swings, noise margins and logic levels. An example would be mixing Schottky TTL and ECL logic families. The concern here is coupling from the TTL signals to the ECL conductors. Since TTL swings 3 volts and the ECL family has only a 100 mV DC noise margin significant undesired coupling can occur.

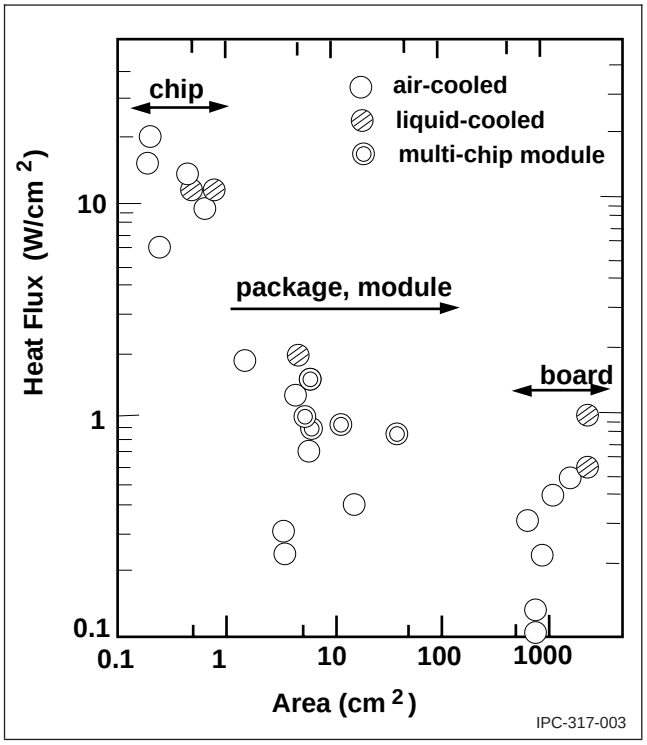


Figure 3 Heat flux vs. component area

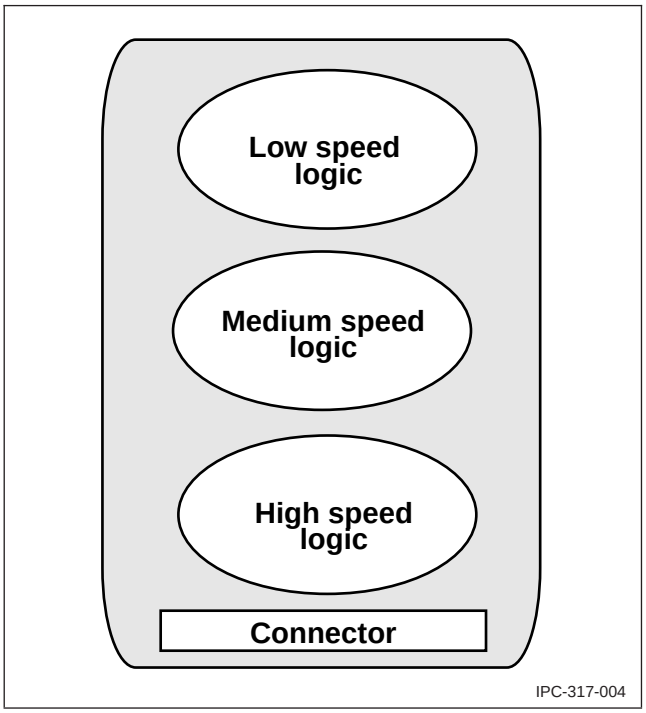


Figure 4 Component placement guideline

When copper planes are used to distribute logic levels, crosstalk (coupling) can also occur through the ground return path for these signals. This is called common mode impedance coupling. Essentially, a returning signal causes a ground potential rise due to the DC resistance of the plane. This problem can be very significant especially in analog circuitry when digital logic is present.

Several techniques can be used to control crosstalk in these environments.

a. Confine logic families geographically.

b. Restrict signal conductors for each logic family to those areas.

c. Provide separate return paths for each logic family.

d. Place components away from I/O connector in descending order of speed (see Figure 4).

e. Terminate controlled impedance conductors to reduce reflections which generate more noise.

f. Restrict conductor parallelism.

g. Specify and control conductor to conductor spacing.

h. Place components close together to minimize conductor lengths and parallelism.

i. Lower the relative permittivity

j. Reduce the signal to ground separation

The impact on circuit board design due to these considerations will include:

a. Circuit board technology must now be capable of managing crosstalk.

b. Multiple power and ground planes required.

c. Added density due to the addition of terminations and tight placement.

d. Selective signal routing criteria.

These can greatly increase complexity and place limitations on the available circuit board technology.

4.4.2 Impedance Control In cases where high-speed signals are being transmitted, the signal conductors may need to be considered as transmission lines. This means, as a minimum, specifying the characteristic impedance of those lines. Since transmission lines should be terminated in their own impedance, a designer must provide for termination resistors.

Specifying a controlled impedance board and providing for termination resistors will add complexity to the design.

a. Termination resistors (one for each signal line) increase density and complexity.

b. Placement should be made so that each signal travels the shortest path from source (first point) to termination. Poor placement can result in very dense signal routing.

c. Circuit board technology must now be capable of controlling impedance.

d. Minimum component to component spacing may eliminate the need for controlled impedance lines but may greatly increase density.

4.4.3 Power Distribution Higher speed devices require the power supply to provide energy quickly. Figure 4 illustrates a typical board placement which shows the highest speed logic near the connector and the lowest speed logic away from the connector (This assumes that power is being provided from off the card). Placement of these devices is not only dependent on performance requirements, but also on thermal requirements and capabilities.

4.4.4 Thermal Management As mentioned, high-speed devices can consume great amounts of power, and consequently dissipate much heat. In the placement of components, the following thermal management techniques should be considered.

a. When possible, ''hot'' components should be spaced apart as greatly as possible.

b. Convection Cooling— Components should be placed such that air flows parallel to component orientation.

c. Conduction Cooling usually involves the placement of a metal 'heat sink' or 'chill plate' on the surface or buried within the board. In these applications, placement must allow for sufficient metal surface area (i.e. usually requires greater component spacing).

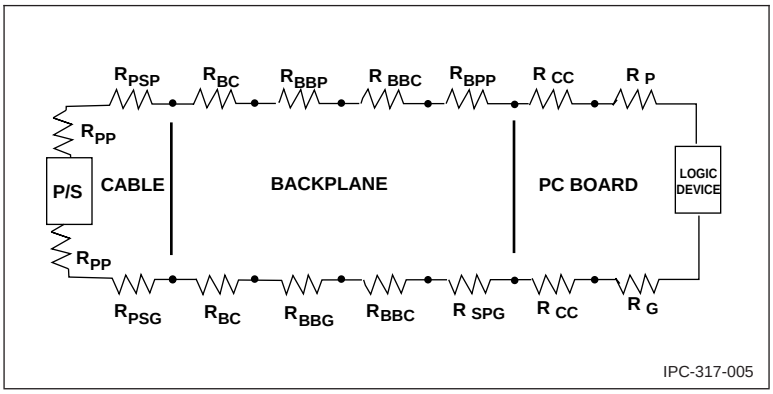


Figure 5 DC distribution model

4.4.5 System Cost Consideration should always be given to the cost of design and manufacturing. Generally, complexity adds density and cost. Cost does not necessarily just mean dollars. Cost can include lead times and reliability. Overspecifying a design ''to be sure it will work'' can significantly impact total cost.

Designing high-speed circuits is rarely a simple matter. There are many factors to take into consideration which usually act in direct opposition to one another.

Placing high-speed components closely together might reduce the need for transmission line parameters and reduce crosstalk problems, but may result in thermal management problems and increase the number of layers in a circuit board (due to increased density). Increasing the spacing will reduce the thermal problems but could add crosstalk and impedance restrictions. We can see that in high-speed design there are many considerations. It is the job of the circuit designer to understand the system specifications and weigh the alternatives to provide the simplest, cost effective, reliable solution for meeting those specifications.

5.0 Electrical Considerations

5.1 Power Distribution This section presents information used for calculating DC and AC noise characteristics for system power distribution. Factors degrading power distribution may be grouped into two major categories; Metallic losses and dielectric losses. Spurious radiation loss is generally negligible.

The DC power distribution system encompasses the system from the output of the power supply to the input of each device. For systems with many cards and supplies a simulation of the interaction of each component is desirable to verify and assist the design effort.

5.1.1 System DC Model The DC distribution model is comprised of lumped resistance for each element in the system. Figure 5 shows the interconnection and the major subsections of the model. This DC model analysis determines the DC voltage drop between the power supply and every integrated circuit location. The major elements in this model are described below.

5.1.1.1 Power Supply To Power Supply Cable (R_{PP}) R_{PP} is the contact resistance of the power supply cable to the power supply output. There is a contact resistance for each cable. This resistance is usually on the order of 10^{-6} to 10^{-3} ohms per series mechanical contact. It is recommended to use a bolt, washer, etc. to keep the voltage drop less than 5 mV.

5.1.1.2 Power Supply Cable/Harness (R_{PSP}, R_{PSG}) This is the resistance due to the interconnection cable or harness from the power supply to the backplane or backplane power distribution busbar. The interconnection can take the form of a cable (circular or flat) or a busbar. R_{PSP} is the resistance of the positive voltage cable. R_{PSG} is the resistance of the power supply ground return cable. Typical resistance for various gauges of copper stranded, rope wound, medium hardness cables at 25°C are listed in Table 1.

5.1.1.3 Power Supply to Busbar Connection (R_{BC}) This is the contact resistance of the power supply cables to the backplane busbar. There is a contact resistance for each cable. This resistance is usually on the order of 10^{-6} to 10^{-3} ohms per series mechanical contact. It is recommended to use a bolt, washer, etc.) to keep the resultant voltage drop less than 5–10 mV.

5.1.1.4 Busbar (R_{BBP}, R_{BBG}) This is the resistance of the backplane power distribution busbars from the power supply

Table 1 Copper Wire Characteristics

Gauge	Number of strands	Diameter (in.)	Area sq. in.	Resistance mΩ/ft.
2/0	19	0.419	0.1045	.08224
1/0	19	0.373	0.0829	.1037
1	19	0.332	0.0657	.1308
2	7	0.292	0.0521	.1649
3	7	0.260	0.0413	.2079
4	7	0.232	0.0328	.2622
5	7	0.206	0.0260	.3306
6	7	0.184	0.0206	.4169
7	7	0.164	0.0164	.5257
8	7	0.146	0.0130	.6629
9	7	0.130	0.0130	.8359
10	7	0.116	0.0082	1.054
12	7	0.092	0.0051	1.676
14	7	0.073	0.0032	2.665
16	7	0.058	0.0020	4.237
18	7	0.046	0.0013	6.738
20	7	0.036	0.008	10.71

Table 2 Copper Busbar Resistances/ft

Cross-section Area (sq. in.)	Resistance (mΩ)
0.1662	.050
0.1318	.063
0.1045	.080
0.0829	.102
0.0657	.128
0.0521	.162
0.0413	.204
0.0328	.257
0.0260	.324
0.0206	.409
0.0164	.515
0.0197	.650
0.0103	.820
0.0082	1.033
0.0065	1.30
0.0051	1.64

cable contact to the backplane contact. R_{BBP} is the positive busbar resistance. A busbar is a metal strip which has a lower resistance than the backplane or circuit board. R_{BBG} is the ground return busbar resistance. For multiple backplane connections this resistance will be modeled as a series of resistances between each backplane connection point. Cross-sectional resistances for copper (99% pure) at 25°C are listed in Table 2.

5.1.1.5 Busbar to Backplane Connection (R_{BBC}) The contact resistance of the backplane busbar to the backplane. This resistance is usually on the order of 10^{-6} to 10^{-3} ohms per series mechanical contact.

5.1.1.6 Backplane (R_{BPP}, R_{BPG}) This is the plane resistance from the busbar contact to the circuit board (daughter card) connector. R_{BPP} is the positive voltage plane resistance. R_{BPG} is the ground return plane resistance. Since most power distribution systems have distributed daughter card contacts R_{BPP} and R_{BPG} will be the resistance between each contact point.

5.1.1.7 Backplane to Daughterboard Connector (R_{CC}) This is the backplane to daughterboard connector pin and contact resistance. This resistance should be the value after a large number of insertions and extractions. For a multiple backplane to daughterboard interconnect scheme the resistance will be broken down into each contact. For lumped connector pin locations, the pin resistances can be paralleled. For two piece connector systems R_{CC} is the total resistance for both connectors.

5.1.1.8 Daughterboard (R_P, R_G) This is the power plane or line resistance for the daughterboard. R_P is the positive voltage plane resistance. R_G is the ground return plane resistance.

5.1.2 Power Plane Impedance The power distribution planes utilized in backplanes and daughterboards do not have zero impedance. Likewise the power supply doesn't have a zero source resistance. A high level model of a multilayer power distribution network is shown in Figure 6.

In the above figure the power supply is represented by a voltage, source V_S, R_{SP}, and R_{SG}. The distribution impedances are broken out as backplane and daughterboard sheet inductances, resistances, and plane-plane capacitance.

5.1.2.1 AC Impedance The power distribution AC impedance is subdivided into three components as shown in Figure 7. The first is the switching transient impedance (Z_{SW}).

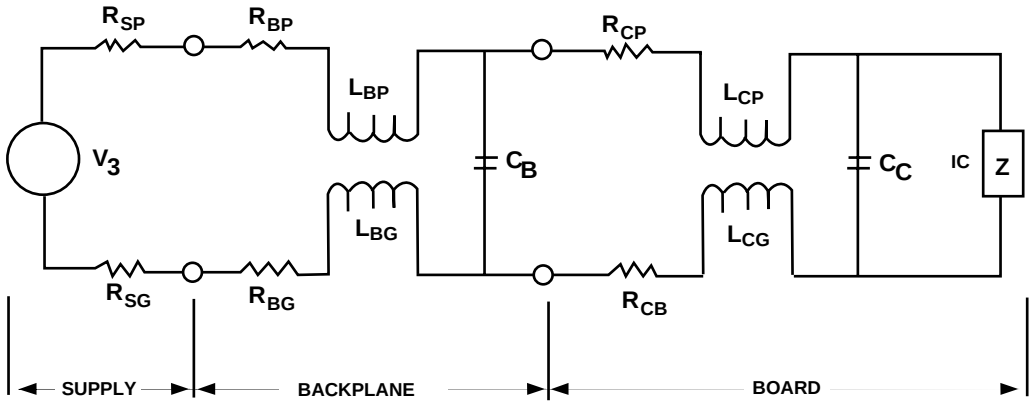


Figure 6 DC power distribution system (without remote sensing)

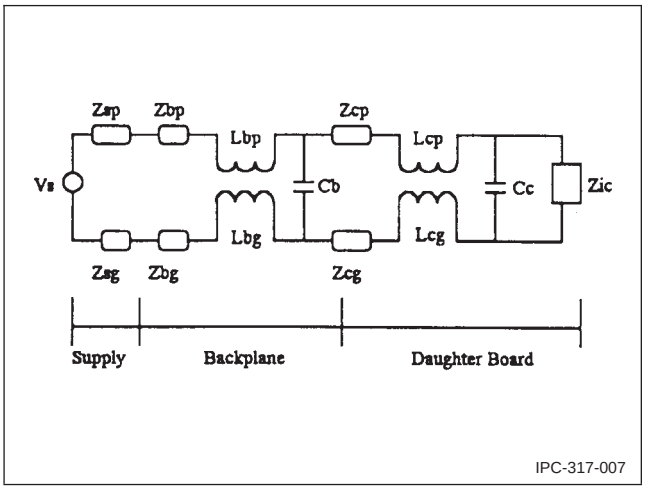


Figure 7 Decoupling impedance model—power supply

This impedance is the interconnect between the closest discrete decoupling capacitor and the component. This impedance can be reduced by using internal power planes that are very close.

The second component is the impedance due to the bulk capacitor charging the IC decoupling capacitors (Z_{BC}). The current in this impedance is lower frequency and higher amplitude than the current in the first component. The voltage drop due to the lower impedance because of the lower frequency involved will be less than the above case.

The bulk decoupling capacitance refresh component (Z_{RC}) is the final element of the circuit board decoupling impedance. This current is responsible for recharging the bulk capacitors. It is supplied from the power supply and will usually have the lowest frequency component of the current.

Each of the board impedance components will be modeled as a transmission line plane-over-plane network. This closely models the worst case configuration because of the regular layout of the printed circuit boards. A brief explanation follows.

The IC's are laid out in regular rows and columns and assuming that every device switches simultaneously then the current will maintain an even distribution as it did in the DC case. The general impedance equation for parallel planes as follows:

$$Zp = SQRT(R_p^2 + (L_p^2 - C_p^2) \quad 5.1)$$

Where L_p = Plane Inductive Impedance
R_p = Plane Resistance
C_p = Plane Capacitive Impedance

5.1.2.2 DC Resistance The static voltage drop between any two points on a copper plane is determined by multiplying the maximum load current by the plane sheet resistance, R_T.

$$R_T = 679 / T_P \ \mu\Omega/\text{square} \quad 5.2)$$

where, T_P = thickness of plane (mils)

A model analysis is used to determine R_T between each integrated circuit location. A computer program can be utilized to simplify the calculations. Each device is modeled as a point load and each connector pin is treated as a point source.

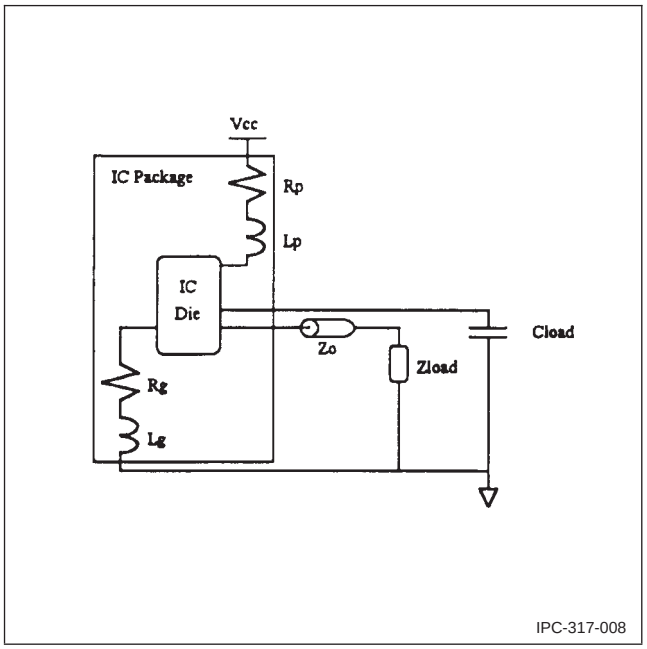


Figure 8 Device decoupling model

5.1.3 Integrated Circuit Decoupling A packaged device must provide sufficient current for its circuitry to operate. This includes high peak current requirements during output switching. The circuit board power system must provide this current without lowering the input supply voltage below its required minimum level.

When the power supply is too far away or the stored energy in the board is insufficient, capacitors are placed near the devices, connected between the power and ground planes to provide this current. In a sense, these capacitors provide the charge current to the device instead of the power planes. The power plane creates a capacitor which can also provide a small amount of high frequency current. These planes should be spaced very close to maximize its capacitance. When they discharge their current into the device they quickly recharge from energy stored in slower discharging capacitors and power supplies in time for the next required discharge.

5.1.3.1 Decoupling Model Figure 8 presents a device decoupling model. Shown are the decoupling capacitor, power planes, signal load, and device models. The device decoupling system is composed of several elements. Every element can be modeled as a network of resistors, capacitors, and inductors. Figure 8 illustrates the interconnection of the following decoupling system components:

- Decoupling Capacitor
- Device Power Lead
- Device Ground Lead
- Transmission Line Load

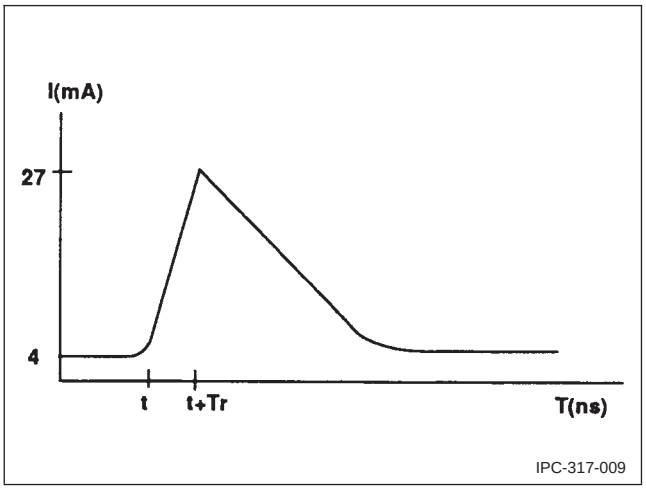


Figure 9 74S00 Typical output switching current

- Capacitive Load – C_L, R_L, L_L
- Power Plane − R_{PL}, C_{PL}

5.1.3.2 Switching Current Frequency Content An integrated circuit has two power supply current components; steady-state bias and output drive. Component data sheet provide these current specifications.

The steady-state bias current is listed over the full temperature and supply voltage specifications. On large devices, such as microprocessors and memories, an average value is provided for power supply size estimation.

The output drive current is typically not specified and must be calculated. Because the signal loads and the device outputs are non-linear, the current is typically best characterized by a time dependent current waveform. Figure 9 presents a typical waveform for a single output of a 74S00 Schottky TTL device.

This waveform shows both the steady-state bias current and output drive current. The 4mA current steady-state level, as shown, raises the entire output switching waveform. As the output switches the current increases at the same rate as the output's risetime. It peaks when the output short circuit current is achieved and decays at a rate based on the output loading characteristics.

The frequency response required by the decoupling capacitor system may be predicted by transposing the time domain waveform into its frequency components using a Fourier Transform. The most critical frequencies are generally the result of the risetime, not just the primary clock frequency.

5.1.3.3 Inherent Plane Electrical Model Section 5.1.2.1 presented the parallel plane impedance of a two plane power distribution system. The power distribution model can be partitioned on a per device basis. In the per device model, the plane inductance (L_P), parallel-plane capacitance (C_P), parallel-plane impedance (Z_P), and plane resistance (R_P) are:

$$L_P = L_G = 0 \qquad 5.3)$$

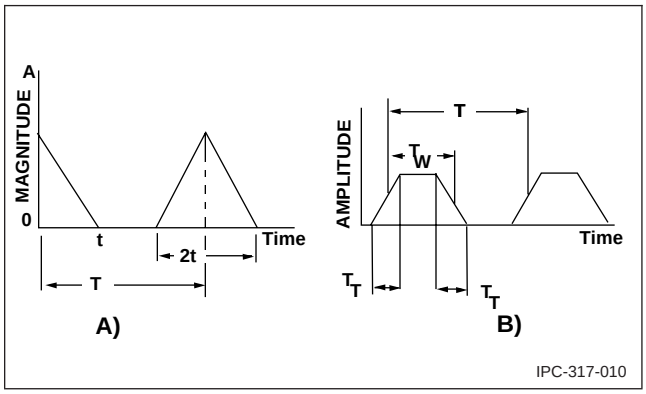


Figure 10 Capacitive and transmission line in current pulses

$$R_P = R_G = R_T \bullet N \text{ ohms [from 5.2]} \qquad 5.4)$$

$$C_P = \varepsilon_r \bullet \varepsilon_O \bullet S / H = 0.225 \times 10^{-6} \bullet \varepsilon_r \bullet S / H \text{ pF} \qquad 5.5)$$

where, R_T = Power plane resistance
N = Number of squares
S = Plane area (square inches)
H = Plane separation distance (inches)

5.1.3.4 Device Output Load Models The signal line load will have two configurations: capacitive line, and transmission line. A capacitive load requires a triangular current pulse at the rate of the output edge transition rate. The current pulse will only occur during the transition.

The transmission line load behaves resistively to the incident signal. The output provides a trapezoidal pulse to the line while the transmission line is active. The I_{cc} requirements have this trapezoidal wave form versus a triangular waveform for a capacitive load. The I_{cc} waveforms for capacitive and transmission line loads are shown in Figure 10. Figure 11 presents the Fourier Transform for the waveform presented in Figure 10.

5.1.4 Decoupling Capacitance Decoupling capacitors provide current to devices until the power supply can respond. High frequency switching, which is composed of a broad spectrum of current frequencies, requires several low to

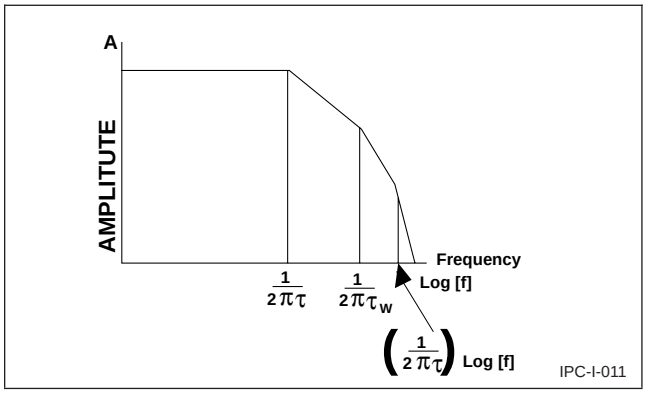


Figure 11 Fourier transform

high frequency capacitors. This is because a single capacitor typically cannot provide such a broad frequency.

5.1.4.1 Switching Transient Capacitance Switching transient capacitance provides very fast energy to charge the output sections of the device during an output transition. This typically is the highest speed content of the waveform and requires the least energy. If insufficient energy is available, the signal transition time will degrade prior to leaving the device package.

In very high-speed devices, the decoupling capacitance may be required to be built into the package to minimize the lead inductance between the capacitance and the device, or located nearby.

When adjacent power planes are provided high speed switching current is provided prior to current being supplied by the discrete decoupling capacitors. This capacitance is increased as the planes are spaced closer together.

5.1.4.2 Line Charging Capacitance Line charging capacitance provides switching current to charge the signal line after the signal reaches the lines. The charge current is required until the line reaches its quiescent state. If insufficient capacitance/ current is provided, the edge transition time will degrade.

Two types of line charging capacitance are required: one for capacitive lines and one for transmission lines. Capacitive line charging requires a relatively slower charging rate than a transmission line, but must provide more current. A transmission line requires a slower, but typically longer pulse to keep the line charged until all of the reflections are over.

When adjacent power planes are provided high speed switching current is provided prior to current being supplied by the discrete decoupling capacitors. This capacitance is increased as the planes are spaced closer together.

5.1.4.3 Low Frequency (Bulk) Capacitance Low frequency capacitance is often termed bulk capacitance. This capacitance is used to recharge power planes and higher frequency charging capacitors, and provide switching current for lower frequency requirements.

5.1.4.4 Capacitor Model Capacitors with shorter leads provide current faster because the lead inductance is much lower. In high-speed designs changing the decoupling capacitors from leaded to leadless SMD capacitors can dramatically increase the circuit performance. The optimum scenario is when the capacitance can be provided within the component package, on the MCM, in the hybrid, or in the circuit board.

The lumped constant equivalent circuit of the capacitor is illustrated in Figure 12. R_{SH} is the insulation resistance and has a value >100 Mohms. It has minimal effect on the operation of the capacitor and will be omitted from further discussions. R_C is the series resistance. L_C is composed of lead and plate inductance. C_C is the bulk capacitance of the capacitor. In a

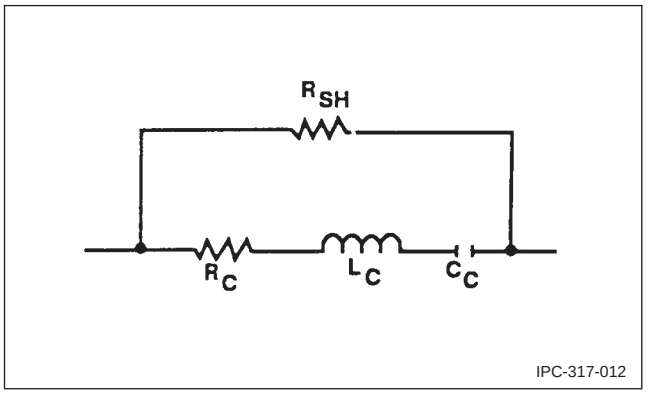


Figure 12 Capacitor equivalent circuit

DIP capacitor the plate inductance is minimal relative to the lead inductance, which is approximately 10 nH/in.

The total effective impedance, Z_C of the capacitor is

$$Z_C = \sqrt{R_C{}^2 + (X_L - X_C)^2} \text{ ohms} \quad 5.6)$$

where, R_C = Series lead and plate resistance

$$X_L = 2 \bullet \pi \bullet f \bullet L_C \quad 5.7)$$

$$X_C = 1/(2 \bullet \pi \bullet f \bullet C_C) \quad 5.8)$$

The series inductance and capacitance yield a resonant frequency at which the effective impedance will equal the series lead resistance, R_C. Below resonance Z_c is dominated by the capacitive reactance. Above resonance Z_c is primarily inductive reactance. Impedance values for 0.1 µF and 0.01 µF DIP and 1206 style capacitors are presented in Figure 13.

5.1.5 Device Power Dissipation The system power dissipation can be calculated by the addition of the component power dissipations. For example, the power dissipation categories are:

1) Bipolar SSI/MSI

2) CMOS SSI/MSI

5.1.5.1 Bipolar SSI/MSI The power dissipation has three primary components:

f	DIP Style				1206 Style			
	0.1 µF		0.01 µF		0.1 µF		0.01 µF	
MHz	X_L	X_C	X_L	X_C	X_L	X_C	X_L	X_C
10	0.6	0.16	0.5	1.6	0.1	0.16	0.1	1.6
100	5.9	0.016	4.7	0.16	1.2	0.016	1.2	0.16
150	8.9	0.011	7.1	0.10	1.9	0.011	1.9	0.10
200	11.8	0.008	9.4	0.08	2.5	0.008	2.5	0.08
300	17.6	0.005	14.0	0.05	3.8	0.005	3.8	0.05
350	20.7	0.004	16.5	0.05	4.4	0.004	4.4	0.05
400	23.4	0.004	18.7	0.04	5.0	0.004	5.0	0.04
L_C (nH)	9.4		7.5		2.0		2.0	
Rc (ohms)	0.065		0.15		0.065		0.15	

Figure 13 Impedance for 0.1 µF and 0.01 µF DIP and 1206 capacitors

1. Iccl and Icch steady state
2. Output load charging
3. Internal dynamic charging

I_{ccl} and I_{cch} Steady State Currents

These values are obtained from the vendor data sheets. For a statistically accurate worst case analysis 10% above typical values used at a 50% duty cycle are used. Or,

$$I_{cc},dc = (1.1/2) \bullet (I_{ccl}, nom + I_{cch}, nom)\ [mA]$$
$$= 0.55 \bullet (I_{ccl}, nom + I_{cch}, nom)\ [mA] \quad 5.9)$$

or,

$$P_{cc}, dc = V_{cc}, nom \bullet I_{cc}, dc\ mW \quad 5.10)$$

Output Signal Load Charging Current

For a worst case analysis use the maximum possible outputs switching at a given time driving their statistically maximum loads. The following decoupling analysis will show that the capacitive load charging current can be approximated as triangular. Thus,

$$I_{cl} = 0.5 \bullet C_L \bullet dVc/dT\ [A] \quad 5.11)$$
$$= 0.5 \bullet C_L \bullet (Voh - Vol)/T_{LH} \quad 5.12)$$

and,

$$P_{CL} = Vout \bullet I_{cl} \bullet N \quad 5.13)$$
$$= (V_{CC}, nom - V_{OH}) \bullet I_{cl} \bullet N \quad 5.14)$$

where, I_{cl} = Load charging current
D_T = Output edge transition rate
C_L = Load capacitance
T_{LH} = LH edge transition rate
P_{CL} = Device power dissipation due to load
N = Number of outputs

Internal Dynamic Charging

As the system clock frequency increases the dynamic power dissipation will increase due to the inherent device capacitance. Vendor data provides the power increase with frequency.

Total Power Requirements

Total power requirement is:

$$P_{TOT} = K_D \bullet (P_{CC}, D_C + P_{CL})\ [W] \quad 5.15)$$
where, K_D = Switching frequency multiplier

5.1.5.2 CMOS Power consumption for CMOS is dependent on the power supply voltage, frequency of operation, internal capacitance, and load. The power consumption may be calculated for each package by summing the quiescent power consumption, $I_{CC}V_{CC}$, and the switching power required by each device within the package. The device dynamic power requirements can be calculated by the equation:

$$P_D = (C_L + C_{PD})V_{CC}^2 f \quad 5.16)$$

5.2 Permittivity

5.2.1 Relative Permittivity The relative permittivity, ε_r, of a substance is defined as the ratio of the permittivity of the material to that of free space. The term relative permittivity is preferred to dielectric constant, since this quantity is not a constant, but varies with several parameters. Factors that influence the relative permittivity of a given material include: the electrical frequency at which the measurement is performed, temperature and extent of water absorption. In addition, if the material is a composite e.g. a reinforced laminate, the value of ε_r may vary enormously as the relative amount of each component of the composite is changed.

5.2.2 Effective Relative Permittivity The effective relative permittivity, ε'_r, is the relative permittivity that is experienced by an electrical signal transmitted along a conductive path. An experimental value of ε'_r may be obtained using a time domain reflectometry (TDR) technique. However, it is frequently more convenient to calculate a value of ε'_r from known values of ε_r.

If a stripline signal conductor is surrounded by a single dielectric that extends to the ground planes, then the value of ε'_r may be equated to that of ε_r for the dielectric measured under the appropriate conditions. However, if more than one dielectric is present between the conductor and the ground planes, a value of ε'_r is determined from a weighted sum of values of ε_r for all the contributing dielectrics. For the purposes of evaluating electrical characteristics of circuit boards, a composite such as a reinforced laminate, with a given ratio of components, is usually regarded as a homogeneous dielectric with an associated relative permittivity.

Some typical electrical configurations are illustrated in Figure 14. For each of the structures: (a) coaxial, (c) stripline and (f) assymetric stripline, if a single dielectric is employed, then the value of ε'_r is taken to be the value of ε_r for that dielectric, but for the remaining structures the situation is more complex.

The microstrip case (c), has a compound dielectric medium consisting of the board material and air. For this configuration, an empirical relationship has been derived (Kaupp, 1967) that gives the effective relative permittivity as a function of the relative permittivity of the board material:

$$\varepsilon'_r = 0.475\varepsilon_r + 0.67 \text{ for } 2 < \varepsilon_r < 6 \quad 5.17)$$

In this expression ε_r relates to values determined at 25 MHz; see the next section for details of frequency dependence.

For electrical configuration (d), the coated microstrip, the following relationship (of unknown origin) is believed to be applicable:

$$\varepsilon'_r = \varepsilon_r \bullet [1 + e^{(-1.55 \bullet H'/H)}] \quad 5.18)$$

H = distance from the reference plane to the signal line
H′ > H + T
H′ is the distance from the reference plane to the top of the dielectric

For the wire-over-ground (b) configuration, if the dielectric

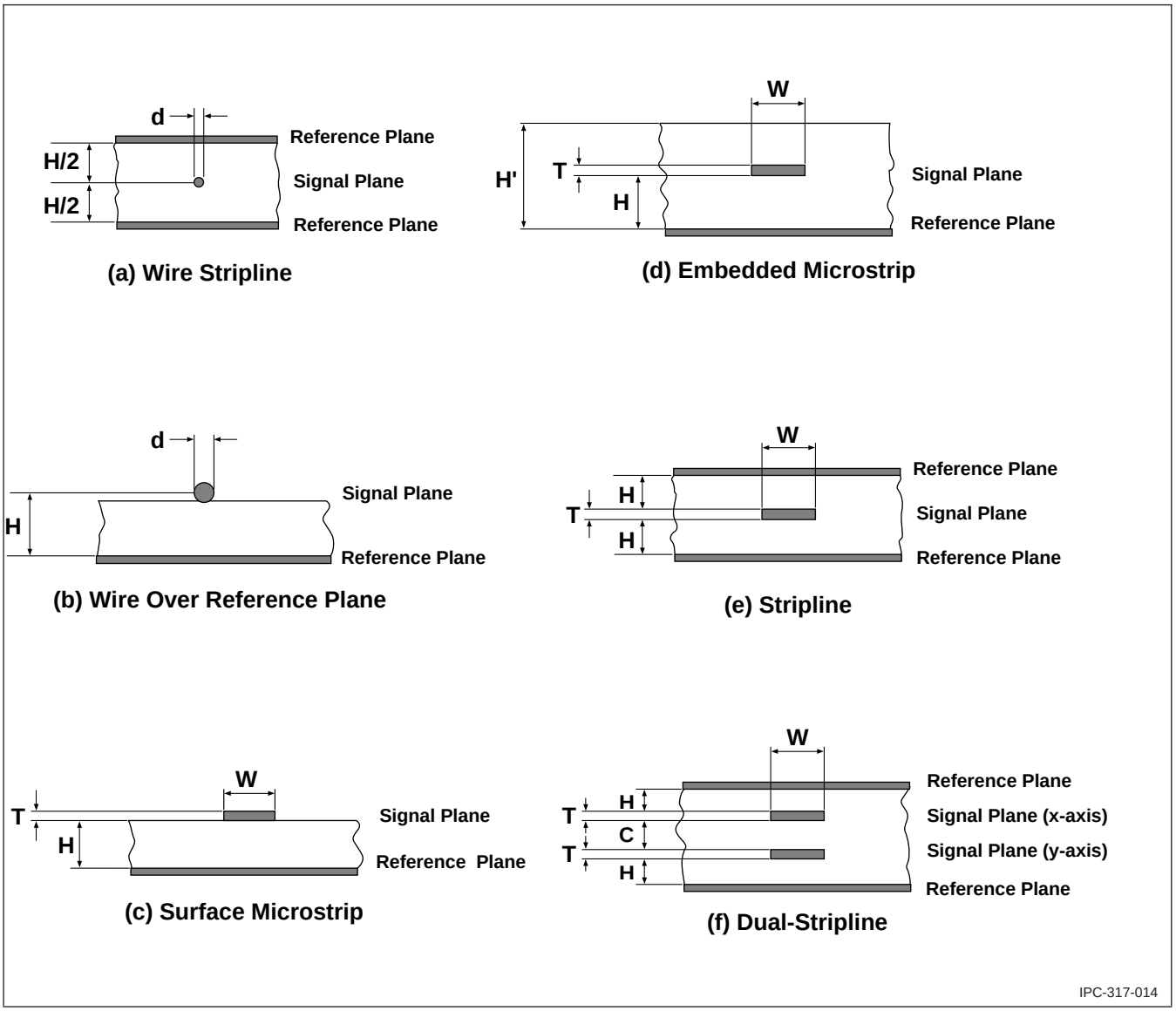


Figure 14 Typical electrical configurations

medium extends from the ground plane beyond the conductor, then the latter expression may be employed. If, however, the dielectric extends only to the level of the conductor, then either the latter expression or the relationship derived by Kaupp may be applied.

Unfortunately, none of the relationships provided in this section are applicable to circuit boards constructed of two or more dielectric materials (excluding air). e.g. Microstrip circuitry coated with solder mask, or printed boards fabricated with more than one type of laminate, or discrete wiring boards with their polyimide insulated wires.

5.2.3 Frequency Dependence As has been explained in the preceding section, values of both ε_r and ε'_r are dependent not only on the material employed, but also on the reinforcement-to-resin ratio (if a composite), temperature, water uptake and the frequency at which the measurement is performed. Once these dependencies are appreciated, steps may be taken to ensure that electrical measurements are performed under conditions that are pertinent to the final application. However, the frequency dependence of ε_r and ε'_r is worthy of further comment, since it is not usually obvious at what frequency measurements should be performed.

Some materials, such as an FR-4 epoxy/glass laminate, exhibit a significant frequency dependence of their dielectric properties, and it becomes important to choose carefully the frequency at which measurements are made. It is essential not only to maintain internal consistency, but also to select the frequency such that the dielectric parameters obtained may be used to provide a precise prediction of the electrical characteristics of the finished circuit board. Since most transmission characteristics for a circuit board are determined by TDR measurements, it is appropriate to use the frequency corresponding to these TDR measurements as the frequency of choice for comparing dielectric parameters. Although TDR is a wideband technique and measurements are performed in

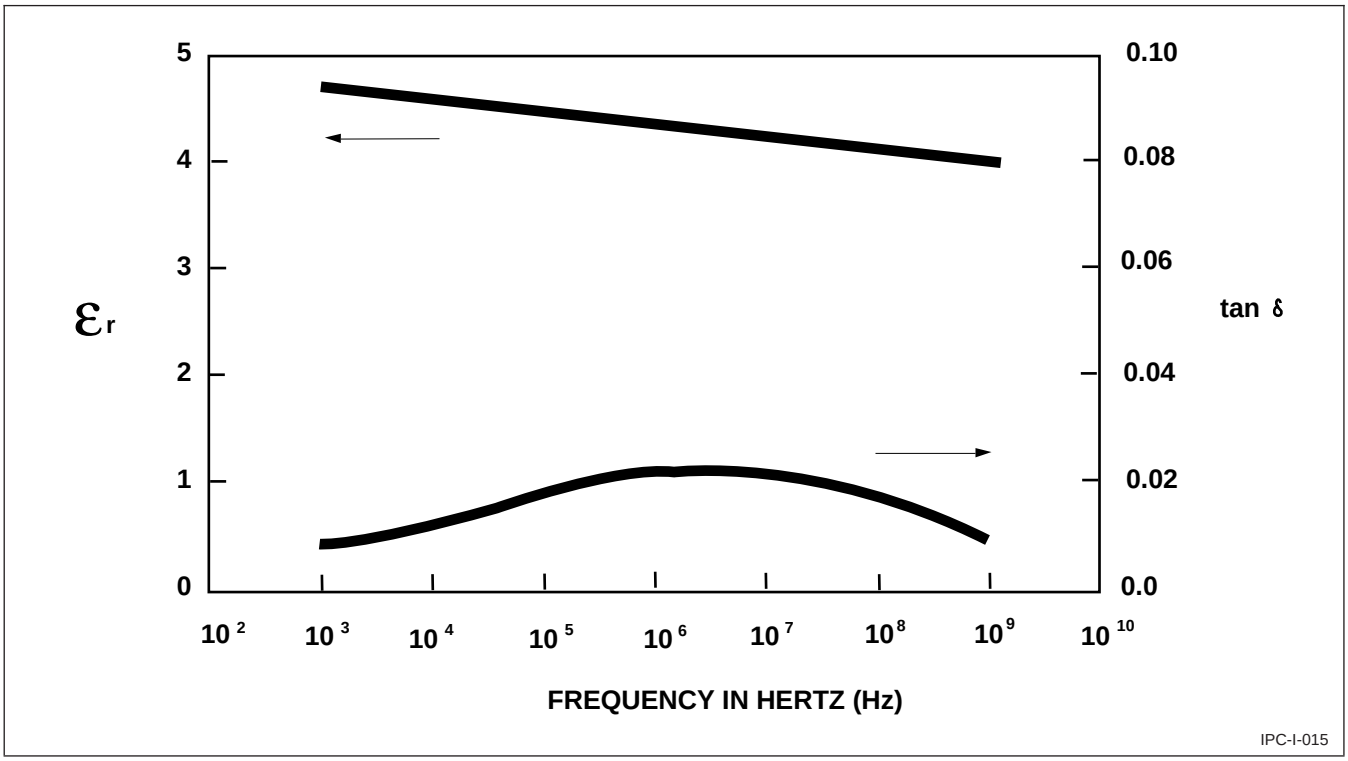


Figure 15 ε_r and tan δ versus frequency for FR-4

the time domain, an approximate frequency may be associated with values determined in this manner. Values of ε'_r, for instance, are determined from the propagation time, but locating the precise position on the TDR output that corresponds to the end of the conductor is frequently subjective. However, if the end point of the conductor is determined in the usual way, from the divergence of two TDR curves recorded with the signal line terminated by an open and a short, then the resulting value of ε'_r corresponds to the highest frequency component of the TDR pulse. The highest frequency of concern, or bandwidth (BW) in Gigahertz, of a digital pulse may be obtained from the relationship:

$$BW\ (GHZ) = 0.35/T_R \qquad 5.19)$$

where, T_R in nanoseconds is the pulse rise time from 10% to 90% of its maximum value. Thus, a typical TDR pulse, with a rise time of 100 ps, has a bandwidth of 3.5 GHz. (Some degradation of this rise time, however, occurs in transmission through the test fixture, thus reducing the effective frequency somewhat.) This dictates that dielectric measurements made by methods other than TDR must be conducted at high frequency.

Figure 15 shows plots of the relative permittivity and loss tangent, measured over the frequency range 1 kHz to 1 GHz, for an FR-4 type laminate with a glass-to-resin ratio of approximately 40:60 by weight. The value of ε'_r for this laminate varies from about 4.7 to 4.0 over this frequency range. This change in the magnitude of ε_r is principally due to the frequency response of the resin and thus is reduced if the proportion of glass in the composite is increased. In addition, the frequency response of ε'_r will also be changed if an alternative resin system is selected. Material suppliers typically quote values of dielectric properties determined at 1 MHz. However, referring to Figure 15, the value of ε'_r (4.4) at 1 MHz is some 10% higher than the more appropriate value (4.0) at 1 GHz. Consequently, use of the 1 MHz value of ε'_r to calculate the propagation time or the characteristic impedance would result in a systematic error of approximately 5%. However, if a dielectric were selected that has a much reduced frequency response, such as PTFE, the question of frequency dependence of dielectric parameters becomes insignificant.

An exception to using high frequency values of ε'_r, to estimate values of ε'_r and subsequently calculate transmission characteristics, occurs when using empirical formulae based on measurements at a particular frequency. This is the case for the relationship given by Kaupp, which is based on measurements made at 25 MHz. Under such circumstances, values of ε'_r should be used that have been determined at a frequency as close as possible to that used in establishing the original expression.

5.3 Capacitive Versus Transmission Line Environment

At low frequencies, a signal path on a circuit board may usually be represented electrically as a capacitance in parallel with a resistance. However, as the frequency is increased, this approach of lumped circuit modeling breaks down and signal paths must be regarded as transmission lines. For transmission line interconnects, the electrical and dielectric properties of the board materials have an enhanced importance and greater care must be taken with the design and termination of

Table 3 Typical Data for Some Logic Families

Logic Family	Typical Rise Time (ns)	Band Width (MHz)	Wavelength in Free Space		Wavelength in FR-4*		Half Rise Dist. in FR-4*	
			m	inch	m	inch	m	inch
TTL	8	44	6.8	268	3.1	122	0.55	21.7
Schottky TTL	3	120	2.5	98	1.2	47	0.21	8.3
ECL	0.6	580	0.52	20.5	0.24	9.5	0.041	1.6
GaAs	0.1	3500	0.086	3.4	0.040	1.6	0.0069	0.27

*Relative permittivity of FR-4 was taken as 4.7

the circuit. Several attempts have been made to define the point at which conductors act as transmission lines; the required analysis being performed in either the frequency or the time domain. However, the critical point to remember for digital signals is that it is the pulse rise time, and not the rate at which the device is clocked, that is a key determining factor. Of course, the clock rate is a dependent parameter since the faster the rise time the faster a device can be clocked.

In the frequency domain, to obtain the point at which a conductor carrying a digital pulse must be regarded as a transmission line, first consider the Fourier components of the pulse and obtain the highest frequency of concern, or bandwidth (BW), from the expression:

$$BW\ (GHz) = \frac{0.35}{T_r(ns)} \qquad 5.20)$$

where T_r is the pulse rise time from 10% to 90% of its maximum value. This band width may then be used to calculate a corresponding wavelength in free space, and a consequently reduced wavelength in the dielectric of interest. A comparison is then made between this later wavelength and the length of the circuit conductor. For digital circuitry, if the circuit conductor length is greater than one seventh of the wavelength then the conductor typically must be considered a transmission line (Figure 16). (For analog circuitry, which is less tolerant of noise, the critical conductor length is usually shortened to one fifteenth of the wavelength in the dielectric medium.) Table 3 lists typical device rise times, the corresponding band widths and wavelengths in air and in FR-4.

However, an alternative equivalent definition of the point at which a circuit board significantly affects the transmission characteristics of a propagating pulse, one that is conceptually more straight forward for digital systems and more widely cited within the circuit board community, compares the rise time to the path length without transforming into the frequency domain. The premise is to determine, for the transmission of a pulse of a given rise time, how long a conductor may be before a significant voltage difference is realized along its length. Conductors longer than this critical value are then regarded as transmission lines. Initially, the rise distance, S_r, in the dielectric of concern is calculated from the device rise time and effective relative permittivity of the medium:

$$S_r(m) = T_r \cdot / \sqrt{\varepsilon_r} \qquad 5.21)$$

where, S_r = Trace Length (m)

T_r = Signal risetime (s)

c = Speed of light

If circuit lengths are equal or greater than half S_r, then the circuit is regarded as a transmission line. i.e., if the maximum voltage drop is greater than half the pulse height value. The choice of $0.5S_r$ to determine the maximum path length before the onset of transmission line characteristics is somewhat arbitrary, but this length is important due to other practical considerations: For path lengths longer than $0.5S_r$, reflections from a mismatched load impedance may be received back at the source after the pulse has reached its maximum plateau value, and pulse additions that occur under these circumstances may lead to false triggering of a device. For path lengths shorter than $0.5S_r$, however, reflected pulses are received back at the source before the pulse has reached its plateau value. Therefore, any modification of the pulse shape will only be to the leading edge, which is less likely to produce false device triggering. Values of $0.5S_r$ are listed in the final column of Table 3. It has been suggested that circuit conductors longer than $0.3S_r$ be regarded as transmission lines and these more stringent criteria allow a greater margin for error. However, irrespective of the precise definition that is used, the point at which a circuit becomes a transmission line is not defined by a single variable, but by the interplay of device rise time, conductor path length and the relative permittivity of the medium. Once we enter the realm of effective transmission line design, close attention must be paid to the models described in the following sections.

5.4 Propagation Delay Time

5.4.1 Capacitive Line When the signal line is considered a capacitive line the propagation time is calculated assuming the line plus the loads connected to it are purely capacitive.

Because the reflections on the short interconnecting line occur several times during the pulses's risetime, the net result is a degradation of the edge transition time, i.e., slowing down, versus distinct steps that occur in transmission lines.

Using the transmission line equations generally provides a much faster propagation time, creating an inaccurate result.

5.4.2 Transmission Line Using Maxwell's equations, it may be shown that the speed of light in a vacuum, c, is related to the absolute permittivity and absolute permeability

of a vacuum, ε_o and μ_o, respectively, by:

$$c = \frac{1}{\sqrt{\varepsilon_0 \mu_0}} \quad 5.22)$$

More generally, for the velocity of propagation, V_p, of a wave in a homogeneous dielectric:

$$V_p = \frac{1}{\sqrt{\varepsilon\mu}} \quad 5.23)$$

where,

ε is the absolute permittivity of the dielectric and
μ is the absolute permeability of the dielectric.

Since the dielectrics employed in the fabrication of circuit boards are not ferromagnetic in nature, μ may usually be taken to be equivalent to μ_o. Consequently, the propagation delay time, T_{PD}, of a signal traveling through a conductor surrounded by a homogeneous, non-ferroelectric medium, is given by:

$$T_{PD} = \sqrt{\varepsilon\mu_o} \quad 5.24)$$

Using equation 5.22 to substitute for μ_o gives:

$$T_{PD} = \frac{\sqrt{\varepsilon}}{c\sqrt{\varepsilon_0}} \quad 5.25)$$

and therefore:

$$T_{PD} = \frac{\sqrt{\varepsilon_r}}{c} \quad 5.26)$$

For a signal passing through a conductor in a circuit board, where more than one dielectric may be present, it is more appropriate to substitute the effective relative permittivity, ε'_r, for ε:

$$T_{PD} = \frac{\sqrt{\varepsilon'_r}}{c} \quad 5.27)$$

It may be seen that propagation delay time is directly proportional to the square root of the effective relative permittivity. In order to calculate the propagation time for a signal transmitted down a specific conductor, one must use the above equation and refer to section 5.2.2 if a value needs to be derived for ε'_r from known values of ε_r for the surrounding dielectrics. Alternatively, one may consult section 5.5.1, which lists a compilation of equations for several circuit configurations.

5.5 Impedance Models The characteristic impedance (Z_o) of a circuit line is analogous to the resistance of a DC circuit (given by Ohm's Law as R=V/I). For a high-speed circuit, the impedance is still the ratio of the driving voltage to the current that flows along the conductor. The critical difference is that in the high-speed case we are interested in the current flow during the very short period of time before the rising edge of the voltage pulse reaches the next board component.

Circuit impedance is important in board design for several reasons. First, applying the definition above, it is apparent that the amount of current that a circuit element (driver) will need to pass along a signal path depends upon Z_o. This is taken into account in the design of ICs, and can affect how receivers may be placed along the circuit. (See Section 5.6 on circuit loading effects.) Second, in high-speed systems, any discontinuity along the path that a signal must travel will cause reflections. Reflections not only reduce the amount of power reaching the receiver, but also may cause ringing along the circuit. These forms of signal degradation can cause systems to malfunction due to missed signals (from attenuation) or due to spurious signals (from reflections).

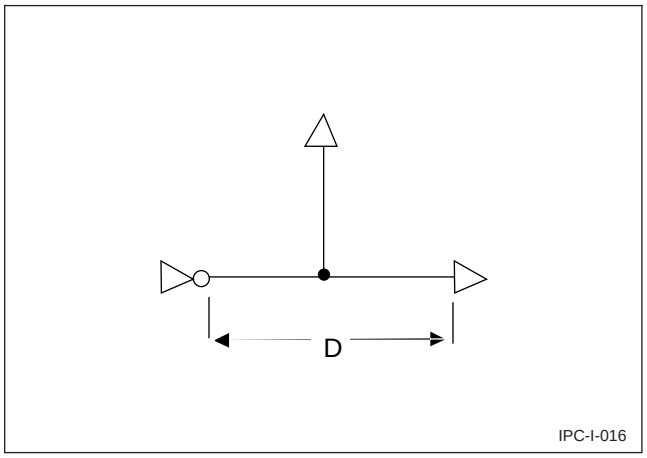


Figure 16 Capacitive loading

Because the time period for measurement is very short (unlike the DC case), circuit termination does not affect the characteristic impedance (although it is very important in determining reflection characteristics). Likewise, the resistivity of the conductor material (typically copper) does not contribute significantly to the high-speed circuit impedance. Both of these effects are because the ratio of driving voltage to current flow (V/I = impedance) is determined before the signal reaches the end of the circuit.

The general formula for the characteristic impedance of a circuit is:

$$Z_o = \sqrt{[\,(R_o + j\,\omega\,L_o)\,/\,(G_o + j\,\omega\,C_o)\,]} \quad 5.28a)$$

where

Z_o = characteristic impedance of circuit in ohms
R_o = resistance per unit length of line [ohms]
L_o = inductance per unit length of line [henrys]
G_o = conductance per unit length of line [mho]
C_o = capacitance per unit length of line [farads]
$j = \sqrt{(-1)}$
$\omega = 2\,\pi\,f$ (f = frequency in Hz)

At high frequencies, it is generally quite accurate to assume that $\omega L >> R$ and $\omega C >> G$, so the equation can be simplified to

$$Z_o = \sqrt{(L_O/C_O)} \quad 5.28b)$$

The following sections will present equations giving specific forms of the above general relation, for each special case. Refer to the figures in section 5.2 for the geometries being

discussed. Refer to Appendix D for typical board constructions.

5.5.1 Microstrip An ''ideal'' microstrip transmission line consists of a narrow conductor separated from an infinite ground plane by a layer of dielectric material. In the simplest case (an ''uncoated'' line), the conductor sits on top of the dielectric, surrounded on the sides and top only by air. We will consider both round and rectangular conductors.

5.5.1.1 Wire The characteristic impedance, in ohms, Z_0, of a single round wire near ground is given approximately by

$$Z_0 = \frac{60}{\sqrt{\varepsilon'_r}} \ell n \left(\frac{4H}{d}\right) \text{ [ohms]} \qquad 5.29)$$

where ε'_r is the *effective* relative permittivity of the medium surrounding the wire (including the space between the wire and ground) while H and d are as defined in Figure 14. A ground is the conductive plane on an adjacent layer.

When no dielectric material is present, $\varepsilon'_r = \varepsilon_{r\ (air)} = 1$. However, for a circuit board, the conductor (wire) is supported from below by a dielectric material, and surrounded above by air. The effective permittivity, ε'_r, is less than the permittivity, ε_r, of the insulating support because the wire is only partially submerged in the support (see Section 5.2). An empirical relationship is

$$\varepsilon'_r = 0.475\ \varepsilon_r + 0.67 \text{ (from 5.17)} \qquad 5.30)$$

Therefore, Equation (5-2a) can be rewritten as

$$Z_0 = 87 \bullet \ell n\ (\ 4\ H\ /\ d) / \sqrt{(\varepsilon_r + 1.41)}\ \text{[ohms]} \qquad 5.31)$$

where ε_r is the permittivity of the material between the wire and ground.

5.5.1.2 Flat Conductor This is the geometry normally found on a printed circuit board as manufactured by copper plating and etching processes. Both the inductance and capacitance (per unit length) are modified from the round conductor case. The capacitance is influenced most strongly by the region between the signal line and adjacent ground (or power) planes. The inductance depends primarily upon an ''effective diameter'' that relates to the perimeter of the circuit.

An article was published over 20 years ago giving an excellent introduction to microstrip transmission lines [Kaupp, 1967]. The author starts with the equation for a wire over ground in air (as given in the previous section). By incorporating theoretical work and experimental measurements he derives the equations describing a rectangular circuit separated from a copper plane by a dielectric layer. (See Figure 14c)

The following equations give the impedance (Z_o) and intrinsic line capacitance (C_o) for microstrip circuitry.

$$Z_o = 87 \bullet \ell n\ [5.98\ H/(.8W + T)] / \sqrt{(\varepsilon_r + 1.41)}\ \text{[ohms]} \qquad 5.32)$$

$$C_o = 0.67\ (\varepsilon_r + 1.41)\ /\ \ell n\ [5.98\ H/(.8W + T)]\ \text{[pF/inch]} \qquad 5.33)$$

For W/H < 1

where

H = Dielectric thickness
W = Line width
T = Line thickness
$0.1 < W/H < 3.0$
$1 < \varepsilon_r < 15$

The radiated electromagnetic signal (EMI) from the lines will be a function of the line impedance, the length of the signal line and the incident waveform characteristics. This may be an important consideration in some high-speed circuitry. In addition, cross- talk between adjacent circuits (see Section 5.7) will depend directly upon circuit spacing and the distance to the power or ground plane.

5.5.2 Embedded Microstrip Line Coated microstrip has the same conductor geometry as the uncoated microstrip discussed above. However, the effective relative permittivity is different because the conductor is fully enclosed by the dielectric material. The equations for embedded microstriplines are the same as in the section on [uncoated] microstrip, with a modified effective permittivity. If the dielectric thickness above the conductor is several mils or more, then the effective permittivity can be determined as in section 5.2. For very thin dielectric coatings, the effective permittivity will be between that for uncoated circuits (previous section) and that for a thickly coated line.

5.5.2.1 Flat Conductor

$$Z_o = \frac{87}{\sqrt{\varepsilon'_r + 1.41}} \ell n \left|\frac{5.98H}{0.8W+T}\right| \qquad 5.34)$$

where

$$\varepsilon'_r = \varepsilon_r\ (1 - e^{\left(\frac{-1.55H_1'}{H}\right)})$$

$0.1 < W/H < 3.0$
$1 < \varepsilon_r < 15$

$$C = [1/(H + T)]\ LN\ [1 - (.6897\ (\varepsilon_r + 1.41)/\varepsilon^{.5})] \qquad 5.35)$$

5.5.3 Stripline A stripline is a thin, narrow conductor embedded between two AC ground planes. Since all electric and magnetic field lines are contained between the planes, the stripline configuration has the advantage that EMI will be suppressed except for lines near the edges of the printed circuit board. Because of the presence of ground planes on both sides of a stripline circuit, the capacitance of the line is increased and the impedance is decreased from the microstrip case.

5.5.3.1 Flat Conductor Stripline parameters impedance (Z_o) and intrinsic line capacitance (C_o) are presented below for flat circuit geometries. The equations assume that the circuit layer is placed midway between the planes.

$Z_o = 60 \bullet \ell n\,[1.9\,(2H+T) / (.8W+T)\,] / \sqrt{\varepsilon_r}$ [ohms] 5.36)

$C_o = 1.41 \bullet \varepsilon'_r / \ell n\,[3.81\,H / (.8W+T)]$ [pf/in] 5.37)

for W/H < 2

where

H = Distance between line and one reference plane
T = Line Thickness
W = Line Width
W/(H-T)<0.35
T/H<0.25

5.5.3.2 Wire

$$Z_0 = \frac{138}{\sqrt{\varepsilon_r}} \ell n \left|\frac{4H}{\pi D}\right| \quad 5.38)$$

where

H = Distance between centerline of wire and one ground plane
D = Diameter of wire

5.5.4 Dual-Stripline In the case that a layer of circuitry is placed between two ground (or power) layers, but is not in the middle, the stripline equations must be modified. This is to account for the increased coupling between the circuit and the nearest plane, since this is more significant than the weakened coupling to the distant plane. When the circuit is placed approximately in the middle third of the interplane region, the error caused by assuming the the circuit to be centered will be quite small.

An asymmetric transmission line closely approximates a stripline except that the signal line is offset from the center line between the power planes. The circuits on one layer are generally orthogonal to those on the other to keep parallelism and cross-talk between layers to a minimum.

5.5.4.1 Flat Conductor Asymmetric impedance Z_o and intrinsic line capacitance (C_o) are presented below.

$Z_o = 80 \bullet \ell n\,[1.9(2H+T)/(.8W+T)] \bullet [1–H/(4(H+C+T))] / \sqrt{\varepsilon_r}$ [ohms] 5.38a)

$C_o = 2.82 \bullet \varepsilon'_r / \ell n\,[2\,(H–T) / (0.268W + 0.335T)]$ [pf/in] 5.38b)

where, B = Height above reference plane
C = Signal plane separation
T = Line thickness
W = Line width
H = Height above reference plane
W/(H-T)<0.35
T/H<0.25

This stackup is shown in Figure 14f. As with stripline, EMI will be shielded except for signal lines near the edges of the AC ground planes. The two signal layers do not electrically interact with each other. This is usually accomplished by making them orthogonal.

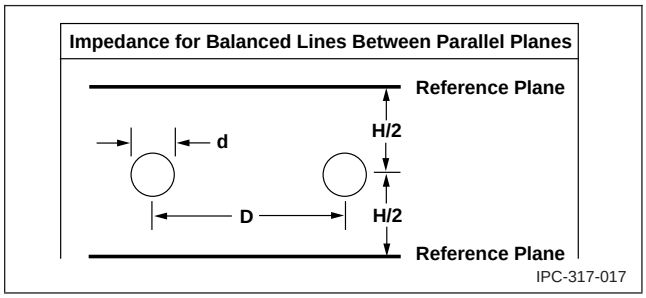


Figure 17

5.5.5 Differential Stripline This is also called a differential pair. It is not the same as dual-strip line, which looks the same in the diagram except that the signal lines in dual-strip line are not necessarily parallel on adjacent planes, but are usually made non-parallel deliberately. Also, with stripline, we are usually concerned with the line-to-ground impedance. Here we wish to find the *line-to-line* impedance for two lines which are routed in parallel on adjacent planes.

5.5.5.1 Flat Conductor Differential stripline impedance Z_o is presented below.

$$Z = \frac{82.2}{\sqrt{\varepsilon_r}} \ell n \left[\frac{5.98C}{.8W + T}\right] \cdot (1 - e^{-.6B}) \quad 5.42a)$$

5.5.5.2 Wire Differential stripline impedance Z_o as shown in figure 17, is presented below.

$Zo = 276 \bullet \log_{10} [\ 4{*}H\ \tanh(\pi D/2H)/\ \pi d]/\sqrt{\varepsilon_r}$ 5.42b)

Where, H = Plane separation
d = Wire diameter
D = Wire center-center spacing

5.5.6 Differential Microstrip Line Differential stripline impedance Z_o as shown in figure 17, is presented below.

$Zo = 276 \bullet \log_{10} [\ (2D/d) \bullet \sqrt{[1+(D/2h)^2]}]\varepsilon_r$ 5.42c)

Where, H = Plane separation
d = Wire diameter
D = Wire center-center spacing

5.6 Loading Effects Signal lines are subdivided into logical interconnect and physical interconnect models. The logical interconnect models define the function of the signal line. The physical interconnect models define physical connectivity of the logic models. The classifications are:

Logical	Physical
> NET	1) Capacitive 2) Transmission line
> BUS	1) Distributed 2) Lumped
> WIRED–AND/OR	1) Radial

A Net consists of a single source and one or more destinations. A Bus consists of multiple sources and one or more

destinations with only one source active at any given time. A Wired-AND consists of multiple sources and one or more destinations with multiple sources active at any given time. These logical configurations will be developed further in section 5.6.5.

5.6.1 Termination Resistors Termination resistors perform two basic functions. The first is to minimize signal reflections caused by a mismatch between the last signal load and the loaded transmission line impedance. Resistors are put in parallel with the load input to match the impedance.

The second method is used with heavily loaded transmission lines. This method uses series resistors. These resistors are connected between the source and the conductor. These resistors slow the rise time of the signal such that reflections won't occur.

5.6.2 Reflections In a transmission line environment the signal is actually an electro-magnetic energy pulse. When the signal travels down the signal line, of impedance Z_O, and reaches a load or line segment of the same impedance, it transfers the entire energy onto it.

If the load, Z_L, has a different impedance, a percentage of the energy pulse is transmitted onto the load and the balance is returned (reflected) back towards the source. The reflected amount can be calculated using a resistive voltage divider concept.

The percent of voltage reflected back towards the source is shown by the load reflection coefficient, ρ_L, where,

$$\rho_L = (Z_L - Z_O) / (Z_L + Z_O) \quad 5.40)$$

The above also holds for the source. If the source impedance differs from the transmission line a percentage of the reflected energy will be reflected back towards the load. The source reflection coefficient, ρ_S, is

$$\rho_S = (Z_S - Z_O) / (Z_S + Z_O) \quad 5.41)$$

5.6.3 Minimum Separation Before a definition of the signal line classifications is presented the concept of minimum load separation is required. This is required because the signal environment definition difference between a lumped load and a distributively loaded transmission line environment is dependent on the spacing at which loads start to affect each other. The minimum load separation distance defines the point at which the reflection from a load on a transmission line begin to affect adjacent loads. In this section a pulse is assumed to have a linear ramp edge transition rate. Exponential rounding at the beginning and end of the transition can be neglected.

In a circuit board environment a logic input has an effective capacitance associated with it. In a transmission line, whenever a capacitive load is attached to the line a point discontinuity occurs. Each of these discontinuities will pass a majority of the incident pulse down the line and a portion of the incident pulse will be reflected back towards the source. The

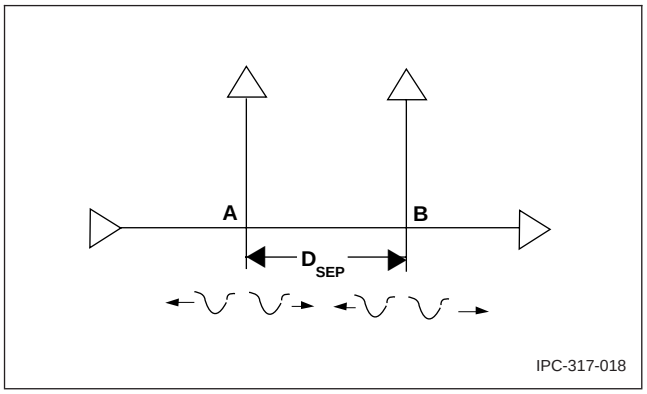


Figure 18 Net illustrating point discontinuity waveforms

width of the reflected pulse is a function of the edge transition rate of the incident pulse.

To isolate the effects of this capacitive load on previous loads there must be a minimum separation distance, L_{SEP}, maintained between adjacent loads such that the reflected pulses will not add up sufficiently to detract from the continuity of the signal. L_{SEP} is calculated in the following manner.

The reflected pulse width is directly equal to the propagation time between points A and B. The two way propagation time between points A and B in Figure 18 is:

$$T_{WA} = 2 \bullet D_{SEP} \bullet T_{PD} \quad 5.43)$$

where, T_{WA} = Width of reflected pulse from A
D_{SEP}= Distance between A and B
T_{PD} = Unloaded line propagation delay

The reflected pulse width, T_{WA}, is expressed by,

$$T_{WA} = 1.7 \bullet T_R \quad 5.44)$$

where, T_R = 10%–90% Edge transition rate

Combining equations 5.40 and 5.41 yields,

$$1.7 \bullet T_R = 2 \bullet D_{SEP} \bullet T_{PD} \quad 5.45)$$

$$D_{SEP} = (1.7 \bullet T_R)/(2 \bullet T_{PD}) = .85\ T_R/T_{PD} \quad 5.46)$$

For a 74Sxx edge transition time of 3.0 nsec and a FR-4 micro stripline propagation time of T_{PD} = 0.148 ns/in.,

$$D_{SEP} = 0.85 \bullet 3.0 / 0.148 = 17.2 \text{ in.} \quad 5.47)$$

Equation 5.44 shows that if the reflected pulse from point B is to have no interaction with point A the loads must be separated by 17.2 inches. This distance between loads is the minimum distance between loads to prevent reflections from overlapping. If the pulses are allowed to overlap and the maximum overlap of the two pulses is limited so the maximum amplitude will be less than the maximum amplitude of either pulse, the minimum separation distance can be reduced without affecting the worst case results. This can be extended to calculate the minimum separation between adjacent loads such that the addition of the reflections from adjacent discontinuities do not exceed the maximum amplitude of either pulse.

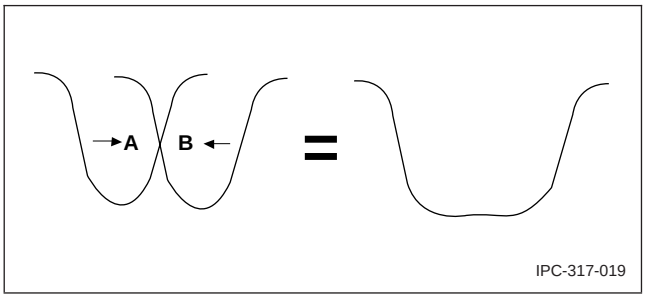


Figure 19 Addition of two pulses traveling opposite directions

As shown in Figure 19 the addition of the two pulses reaches the maximum amplitude and width when one-half of the pulse from A coincides with one-half of the pulse from point B (assuming the load characteristics of point A are equal to point B). Using equation 5.41.

$$D_{SEP} = 0.5 \bullet 0.85 \bullet T_R/T_{PD} = 0.425\ T_R/T_{PD} \quad 5.48)$$

for, T_R = 3.0 ns and T_{PD} = 0.148 ns/in. D_{SEP} = .425 • 3.0 / .148 = 8.6 in. 5.49)

Equation 5.44 shows that if the loads are separated by more than 8.6 inches for 74Sxx devices a LOADED transmission line environment will not exist. The effective transmission line impedance will not be affected. The capacitive loads will generate non-coherent pulses on the transmission line.

Edge transition times, thus propagation times, will be affected due to the energy loss as the pulse travels by each disjoint capacitive load.

The following sections assume that loads are connected at intervals less than the minimum separation distance unless otherwise specified.

5.6.4 Distributed Loading A distributively loaded line is a transmission line where the separation between loads or load clusters is less than the minimum separation distance (equation 5.43). The loads can be evenly or unevenly distributed along the line (see Figure 20).

The transmission line lumped element model simulates the line as a series inductor and parallel capacitor. Each load is treated as a capacitor for AC analysis. The load input resistance is usually neglected due to its high value relative to the line impedance.

Main line is defined to be the conductor between the source and the furthest load. The length of the main line will be the signal line length. All loads that attach in-between the source and furthest load are connected with a line called stubs. As stated above, if the stub length meets the requirements the inherent capacitance of the stub must be included as part of the load capacitance.

When the loads are distributed along the transmission line the effective capacitance per unit length is increased. This will affect the propagation delay and line impedance as follows:

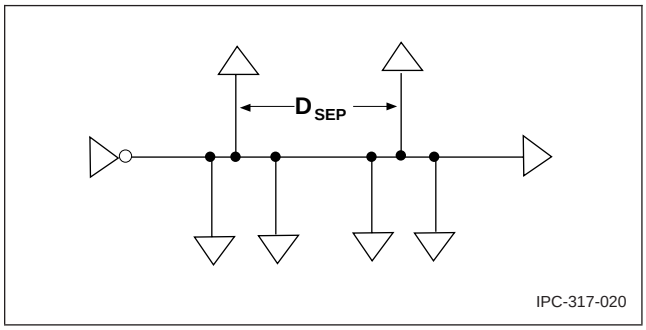


Figure 20 Distributed line

$$C_D = N \bullet C_{IN} \quad 5.50)$$

$$C_L = D_M \bullet C_0 \quad 5.51)$$

$$Z = \sqrt{[L_D/(C_D + C_L)]} \quad 5.52)$$

$$Z'_O = \sqrt{(L_D/C_D)} \bullet \sqrt{[1/(1 + C_L/C_D)]}$$

$$= Z_O / \sqrt{(1 + C_L/C_D)} \quad 5.53)$$

where, C_D = Total load capacitance
C_D = Total line capacitance
Z_O = Loaded line impedance
N = number of loads
C_{IN} = Single load capacitance
D_M = Main line length
L_D = Total line inductance
C_O = Line capacitance per unit length
Z'_O = Effective line impedance

and $T_{PDL} = T_{PD} \bullet \sqrt{(1 + C_L/C_D)}$ 5.54)

where, T_{PD} = Propagation delay-time per unit-length

Each load connection to the main line should have a stub less than 1/4 of the minimum separation distance. This will minimize the noise on the main line. The length and inherent capacitance of the stub must be included as part of the load capacitance value used for C_{IN} and C_L in the above equations.

Example: Transmission line is a microstripline with loads that are distributively attached. Stub lengths = 0 in.

b_M = 10.0″	Z_O = 50 ohms
C_O = 2.0 pf/in	T_{PD} = 0.148 ns/in
C_{IN} = 5.0 pf	N = 6 loads

From 5.50, $C_L = 6 \bullet 5 = 30$ pf

From 5.51, $C_D = 10 \bullet 2 = 20$ pf

$$Z_O = 50/\sqrt{(1 + 30/20)} = 31.6 \text{ ohms}$$

And,

$$T_{PDL} = .148 \bullet \sqrt{(1 + 30/20)} = .234 \text{ ns/in}$$

Where T_{PDL} = propagation delay due to capacitive loading.

As shown in this example the loading can greatly influence the final loaded line impedance. In some instances a minimum

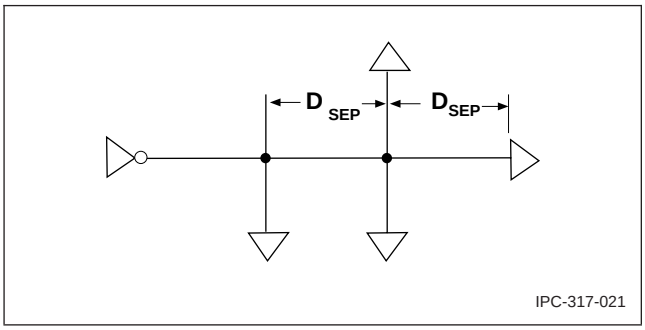


Figure 21 Lumped loading

loaded line impedance is required to keep the first signal plateau beyond required threshold value.

N/D_M is called the maximum loading density. This value will yield the maximum loads per unit length that will maintain Z_O above the minimum pre-defined value.

$$N/D_M = [(Z_0/Z'_0)^2 - 1] \bullet \frac{C_0}{C_L} \qquad 5.55)$$

5.6.5 Lumped Loading A lumped loaded line is a transmission line whose separation between loads is greater than the minimum separation distance (equation 5.41) (see Figure 21). A transmission line environment disappears when lines become heavily loaded near the source causing the signal edge transition time to increase. A lumped load may be a single load or a cluster of loads at any given point.

A load cluster (see Figure 22) consists of multiple loads that are connected to the same point by stubs (star configuration), or a section of the line where several loads are connected as distributed loads.

Lumped loads configured as short distributed lines behave as discontinuities to the transmission line. A series of loads that are within the minimum separation distance will create a distributively loaded transmission line, Z_O. If this section of the transmission line has a length less than $T_R/(2 \bullet T_{PD})$, the loads will be treated as a lumped capacitive load.

If the length is greater than $T_R/(2 \bullet T_{PD})$, the section will be treated as a distributed line and the propagation characteristics will be handled as such.

A TTL/MOS load is modeled as a capacitive load. This capacitive load presents a point discontinuity to the transmission

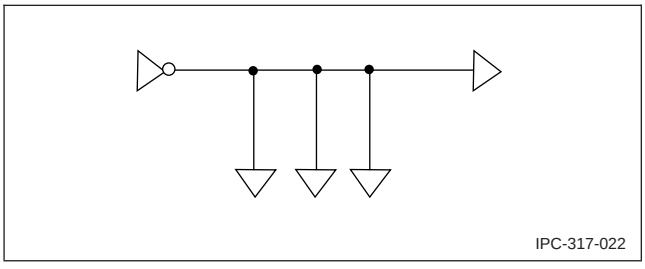


Figure 22 Short distributively loaded cluster

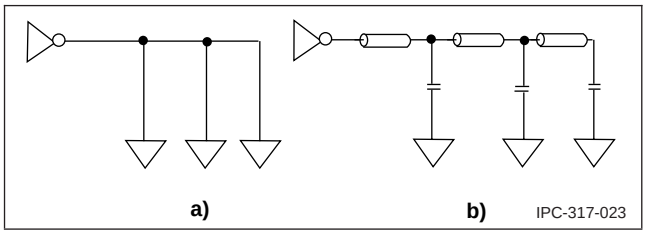


Figure 23 a) Lumped loaded transmission line b) Equivalent model

line. The load is modeled as a Thevinin equivalent capacitor and resistor as shown in Figure 23.

Since the reflections from each point load are not additive the propagation delay will not be affected except for energy losses that occur as the waveform passes. Reflections will show up as ''glitches'' in the waveform, as shown in Figure 24 and will have a magnitude of

$$V_R = C_L \bullet Z_O \bullet V_A / (2 \bullet T_T) \qquad 5.56)$$

where, V_R = Reflected voltage
C_L = Node capacitance
Z_O = Line impedance
V_A = Incident pulse amplitude
T_T = Edge transition time

Additional propagation delay is injected as a result of the time constant, T_{DL}, of the load. For loads whose equivalent resistance, R_L, cannot be neglected equation 5.57 presents its effect on the edge transition rate.

$$T_{DL} = (R_L \bullet Z_O \bullet C_L)/(R_L + Z_O) \qquad 5.57)$$

If there is not termination resistance or R >> Zo the additional propagation delay is,

$$T_{DL} = Z_O \bullet C_L \qquad 5.58)$$

Equation 5.53 will be used as a first order approximation for timing analyses.

Example: Microstrip transmission line is lumped loaded at end with 6 loads. See Figure 25.

D_M = 10.0″	Z_O = 50 ohms
C_O = 2.0 pf/in	T_{PD} = 0.148 ns/in
C_{IN} = 5.0 pf	N = 6 loads
R_L = 10K	

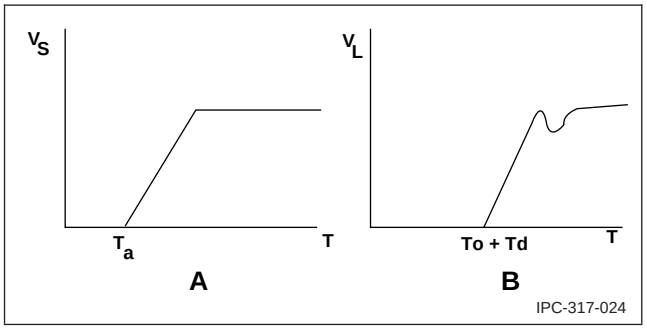


Figure 24 Waveforms for a lumped capacitive load

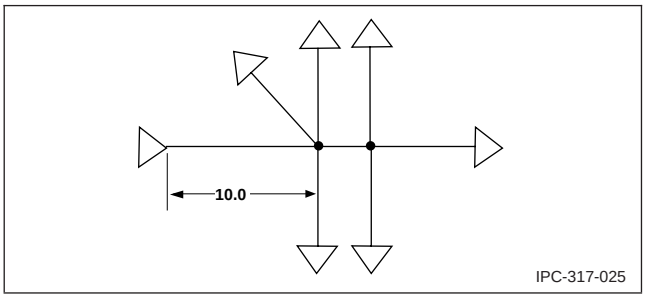


Figure 25 Lumped transmission line

From 5.50, $C_L' = 5.0 \bullet 6 = 30$ pf

From 5.53, $Z_O = 50/\sqrt{[1+0/(10 \bullet 2)]} = 50$ ohms

From 5.54, $T_{PD} = 10 \bullet 0.148 = 1.48$ ns

From 5.57, $T_{D_L} = (10^4 \bullet 50 \bullet 30x15^{12})/4$
$= 1.5$ ns

From 5.58, $T_{D_L} = 10 \bullet 30x10^{-12} = 1.5$ ns

T_D, line $= T_D + T_{D_L}$ 5.59)
$= 1.48 + 1.5$
$= 2.98$ ns

5.6.6 Radial Loading A radial load is a stub of sufficient length and loading that generates a pulse greater than the noise budget and affects the input of another load. The worst case interference will be when a load is located at the junction of the radial line to the main line.

Radial loading occurs when multiple lines diverge from a common point on a line. The divergence point can be located at the source output or at any point along the transmission line, as shown in Figure 26.

As defined above, radial loading occurs when multiple lines diverge from a common point on the main line. Each of these lines have a length greater than the minimum separation distance. Each radial line can be individually treated as a distributed, lumped, or unloaded transmission line dependent on its loading characteristics.

As shown in Figure 27, when a pulse is propagating down a transmission line equal to Z_O and it hits a radial line contact point the effective impedance at that point is $Z_O/2$ (assuming the radial line has an impedance equal to Z_O). If the impedance of the main line and the radial line are equal the pulse will split evenly and 1/3 will travel down each line, and 1/3 is reflected back towards the driver.

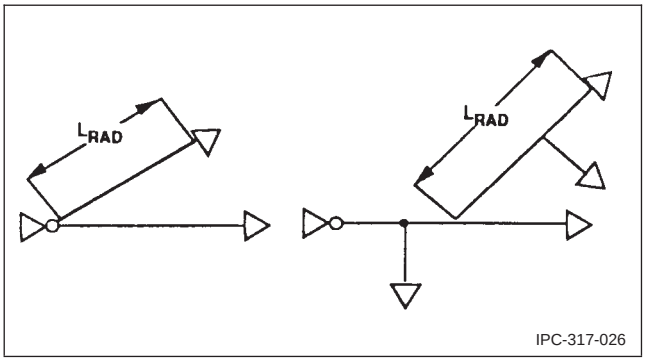


Figure 26 Radial loading

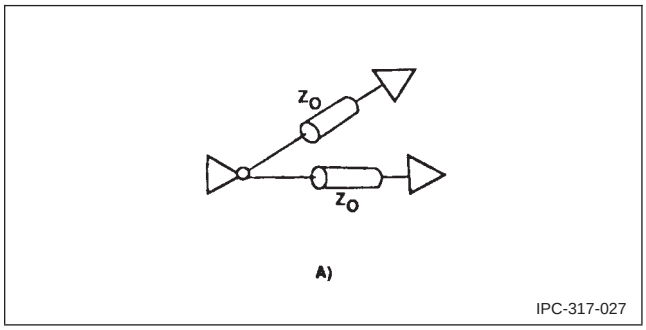


Figure 27 a) Example configuration

Radial lines affect the propagation characteristics of the transmission line by creating the impedance Z_{RAD} at that point. Where,

$Z_{RAD} = Z_O/N$ 5.60)

where, N = Number of radial lines

Each incidence of a radial line will divide the pulse even further. Rules governing system layout must limit the number of radial lines on any given signal line to two. This, coupled with distributed loading effects of the radial and main line will maintain a manageable transmission line environment.

The propagation time for a radial line will be mostly affected by the interaction of the radial line and the main line (see Figure 28). Recall that for the main line, Dm is the distance between the driver and the furthest load. If the net impedance of the intersection results in the signal to drop below threshold for a Low- to-High transition or rise above threshold on a High-to-Low transition the signal line timing will be affected.

The most prevalent implementation of a radial line structure is that of a multiple driver signal line.

Example: Microstrip transmission line, distributively loaded

D_M	= 14.0 in	D_{RAD}	= 6 in
C_O	= 2.0 pf/in	T_{PD}	= 0.148 ns/in
C_{IN}	= 5.0 pf		

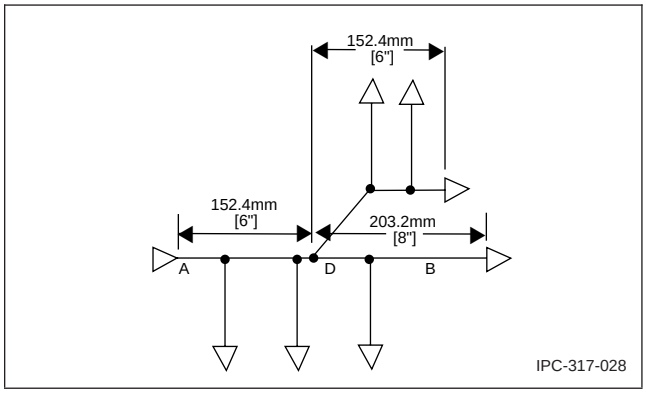


Figure 28 Radial line example

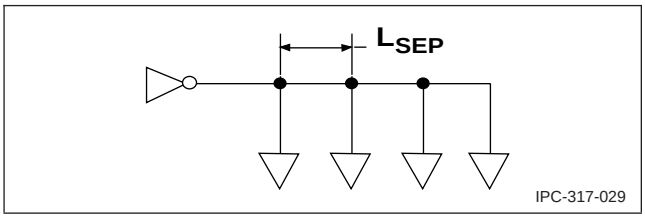


Figure 29 Net configuration

Z_O = 50 ohms

$C_{L,\ main}$ = 4 • 5 = 20 pf

$C_{D,\ main}$ = 14 • 2 = 28 pf

$C_{L,\ radial}$ = 3 • 5 = 15 pf

$C_{O,\ radial}$ = 6 • 2 = 12 pf

From 5.50,

$Z'_{O,\ main} = 50/\sqrt{(1 + 20/28)} = 38.2$ ohms

$Z'_{O,\ radial} = 50/\sqrt{(1 + 15/12)} = 33.3$ ohms

At point D the impedance is

$Z_{O,\ parallel}$ = (33.3 + 38.2)/(33.3 • 38.2) 17.8 ohms

From 5.49,

$T_{PD,\ main} = 0.148 \bullet \sqrt{(1 + 20/28)} = 0.194$ ns/in 5.61)

$T_{PD,\ radial} = 0.148 \bullet \sqrt{(1 + 15/12)} = 0.222$ ns/in 5.62)

Thus,

$T_{D,A-B}$ = 14 • .194 = 2.72 ns 5.63)

$T_{D,A-D}$ = 6•.194 + 6•.222 = 2.5 ns 5.64)

5.6.7 Logic Signal Line Loading Models

5.6.7.1 Net A net is a single source multiple destination signal line, Figure 29. Timing analysis is performed dependent on the load configuration of the net.

5.6.7.2 Bus A bus is a multiple source multiple destination signal line, as shown in Figure 30. Only one source may be active at any point in time. The sources may be a combination of tri-state and open-collector devices.

For timing analyses all of the physical configurations must be analyzed. The first analysis involves the distributed line analysis.

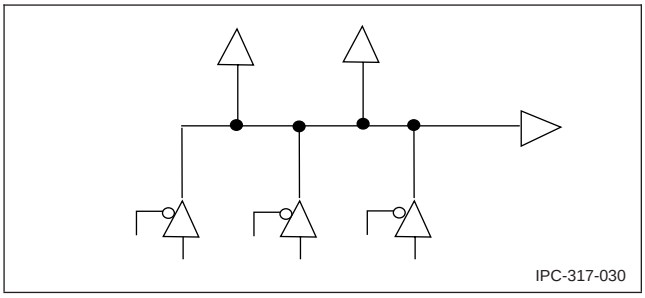


Figure 30 Bus configuration

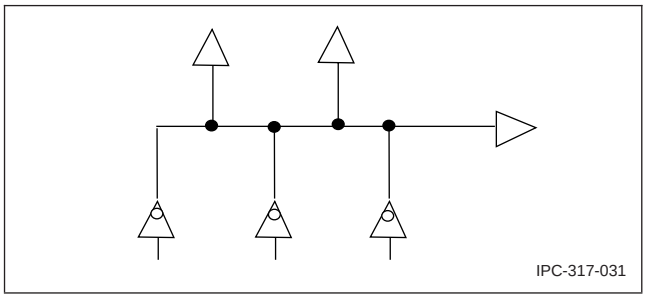


Figure 31 Wired-AND configuration

Termination resistors must be attached to the bus based on the results of the above analyses. Due to the complexity of resistor placement the procedure for termination placement will not be analyzed. It is sufficient to state that the resistors should be placed at locations that will reduce the load impedance such that unwanted reflections and back-porching will be limited.

5.6.7.3 Wired – AND/Wired – OR The wired-AND and wired-OR configuration, Figure 31, is a multiple source multiple destination bus which can have greater than one source active at a given point in time. Sources connected to the line must have open-collector output structures with a pullup/termination resistor network.

Use of wired-AND and wired-OR circuit configurations is nonpreferred and should be avoided if possible. Use of a multiple source, multiple destination bus with the potential for more than one source to be simultaneously active complicates fault-isolation and repair operations significantly.

5.6.8 Timing Calculations This section presents two commonly used models for determination timing effects of a loaded transmission line on the output of the driving impetus.

5.6.8.1 Bergeron Plot The graphical method of finding the transients in a transmission line terminated by nonlinear resistances originates from Bergeron. Its use is illustrated here on a transmission line interconnecting two TTL inverters as shown in Figure 32a.

In Figure 32a, the output of a TTL inverter is connected to the input of a second one by a transmission line with a characteristic impedance of Z_O = 50 ohms and a propagation delay of T_O. Typical voltage-current characteristics of the TTL inverters are shown in Figure 32b. When the output of the first inverter is logic 0, the static operating point is given by the intersection of the V_{out} VERSUS I_{out} for logic 0 output curve with the V_{in} VERSUS I_{in} curve, and is marked as point ''0''. Similarly, when the output of the first inverter is logic 1, the static operating point is given by the intersection of the V_{out} VERSUS I_{out} for logic 1 output curve with the V_{in} VERSUS I_{in} curve, and is marked as point ''1''.

We first find the transients for the case when the output of the first inverter changes from logic 0 to logic 1 at time t = 0. For

times t<0, V_{out}, V_{in}, I_{out}, and I_{in} are given by point ''0'' in Figure 32b. At time t = 0, the output of the first inverter changes to logic 1 and as a result V_{out} and I_{out} instantaneously move from point ''0'' to somewhere onto the V_{out} and I_{out} curve. Hence V_{out} and I_{out} will each change by some amount. We designate these changes by ΔV_{out} and ΔI_{out}, respectively. The output of the first inverter is connected to the left end of the transmission line, thus a signal characterized by ΔV_{out} and ΔI_{out} starts traveling to the right. However, for a signal traveling to the right the ratio of the change in voltage to the change in current is Z_O, that is, $\Delta V_{out}/\Delta I_{out} = Z_O$. This relation now constrains the new point of V_{out} and I_{out} on the V_{out} VERSUS I_{out} for logic 1 output curve to be in a direction with respect to point ''0'' such that $\Delta V_{out}/\Delta I_{out} = Z_O$ = 50 ohms. This constraint is satisfied by a straight line with a slope of 50 ohms drawn through point ''0''. Thus, the intersection of this straight line with the V_{out} VERSUS I_{out} for logic 1 output curve, shown as point A in Figure 32c, determines V_{out} and I_{out} for times 0 <, t<$2T_O$.

The signal that is traveling to the right and that is characterized by a change from point ''0'' to point A in Figure 32c reaches the right end of the transmission line at time t = T_O. As a result, at time t = T_O, V_{IN} and I_{in} will move from point ''0'' to another point somewhere onto the V_{in} VERSUS I_{in} curve. V_{in} and I_{in} at this point, which we denote point B, are each composed of three constituents: the initial conditions given by point ''0'', the incident signal given by ΔV_{out} and ΔI_{out}, and a reflected signal which we characterize by ΔV_{in} and ΔI_{in}. The sum of the initial conditions given by point ''0'' and of the incident signal given by ΔV_{out} and ΔI_{out} is represented by point A. Thus, the difference between point B and point A represents the reflected signal, which is characterized by $\Delta V_{in}/\Delta I_{in} = -Z_o$ = –50 ohms. Hence, point B can be found as the intersection of the V_{in} VERSUS I_{in} curve with a straight line that originates from point A and that has a slope of –50 ohms (see Figure 32c).

The reflected signal characterized by ΔV_{in} and ΔI_{in} reaches the left end of the transmission line at time t = $2T_o$ and will change V_{out} and I_{out} from point B to some other point on the V_{out} VERSUS I_{out} for logic 1 output curve: We designate this new point as point C. By using a reasoning similar to that above, we can show that point c can be found as the intersection of the V_{out} VERSUS I_{out} for logic 1 output curve with a straight line that originates from point B and that has a slope of 50 ohms. The process may also be continued to obtain additional points, as shown in Figure 32c for points D, E, and F. Figure 32c also indicates that as the number of points is increased, they approach the final static operating point, point ''1'', as expected.

The diagram of Figure 32c contains all information required for plotting V_{out}, I_{out}, V_{in} and I_{in} as functions of time. The output of the first TTL inverter changes from logic 0 to logic 1 at time t = 0, hence, V_{out} and I_{out} change from their initial values given by point ''0'' to the values given by point A at time t = 0. The projection of point ''0'' onto the vertical axis provides the initial value of V_{out} (t<0) = 0.15 V, and the projection of point ''0'' onto the horizontal axis provides the initial value of I_{out} (t<0) = –1.5 mA.

Continuing the reference to Figure 32d, for times 0<t<$2T_O$,the projection of point A onto the vertical axis provides V_{out} (0<t<$2T_O$) = 1.3 V, and the projection of point A onto the horizontal axis provides I_{out} (0<2<T_O) = 22 mA. Further values of V_{out} and I_{out} can be similarly found from points C and E as shown in the left two graphs of Figure 32d.

Referring to the right 2 graphs of Figure 32d, at the right end of the transmission line, V_{in} and I_{in} remain at their values given by point ''0'' until Time t = T_O, that is, V_{in} (t= 0.15 V and I_{in}(t T_O) = 1.5 mA. For times T_O < t < $3T_O$, the values of V_{in} and I_{in} are given by the projections of point B as V_{in}(T_O < t < $3T_O$)= 2.35 V and I_{in} (T_O< t< $3T_O$) = 0.5 mA. Further values of V_{in} and I_{in} are obtained from points D and F and are shown in the right two graphs of Figure 32d.

The transients in the circuit of Figure 32a were determined in Figures 32c and 32d for the case when the output of the first TTL inverter changes from logic 0 to logic 1. The transients can be found in a similar manner for a change from logic 1 to logic 0: This is shown in Figure 32e.

5.6.8.2 Lattice Diagram Implementation of the reflection waveform can be achieved with the following tabular approach. This approach is called the lattice diagram. Use the figure in Figure 33 for reference.

The lattice diagram is initiated by drawing the signal line under evaluation with the source on the left and the load on the right. The output of the source is labeled A and the input of the load B. Vertical lines are then drawn below points A and B. These lines indicate the difference in length, D and propagation time $D \bullet T_{PD}$ (T_D).

The first calculation step is to determine the reflection coefficients ρ_s and ρ_L.

Next determine the initial condition of the line. This will be the steady state voltage Vdc.

where, $V_{DC} = V_S(0–) \bullet R_L / (R_L + R_S)$ V 5.65)

At time T+0, Vs has transitioned (since T_T = 0 ns) and the voltage at point A will be determined by equation 5.58. VB will still be equal to Vdc. At T = T_D, V_B is

$$V_B = V + V_{DC} = \rho s \bullet V_L + V_{DC} \quad 5.66)$$

Each reflection for T = $2 \bullet T_D$ to $N \bullet T_D$ will follow the same pattern as above. The process continues until the steady state voltage is obtained.

Characteristics of the Lattice Diagram are:

- Linear, time invariant resistance must be used
- Method is long and tedious to perform by hand
- Easily converted into a computer program
- The resultant waveforms at the load and driver end of the signal line are shown in Figure 34.

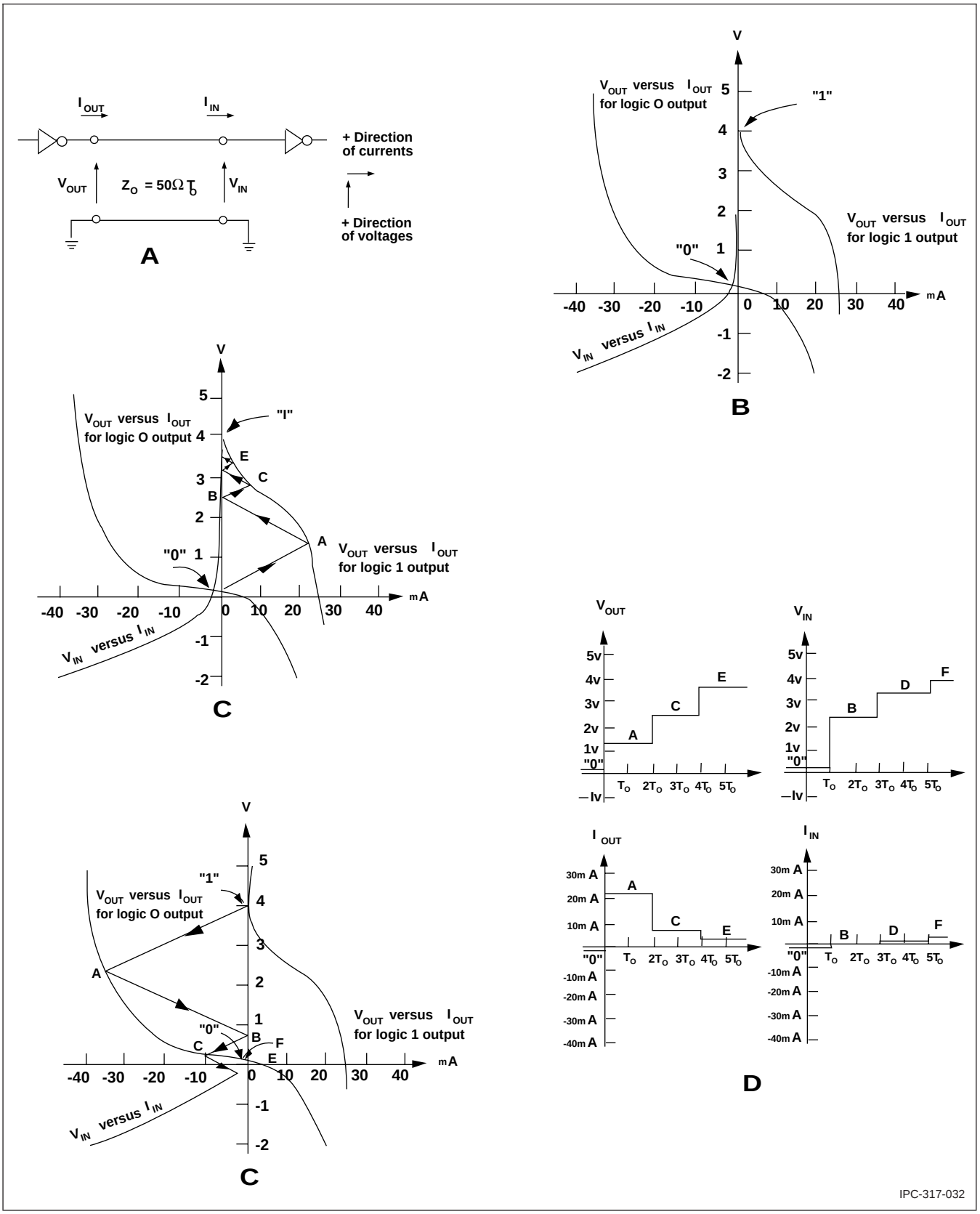


Figure 32 Multiple reflections in a transmission line between two TTL inverters. (a)The circuit; (b)typical static characteristics of the TTL inverters; (c)transition from logic 0 to logic 1 in the voltage-current plane; (d)v_{out}, I_{out}, V_{in}, and I_{in} as functions of time for a transition from logic 0 to logic 1; (e)transition from logic 1 to logic 0 in the voltage-current plane; (f)V_{out}, I_{out}, V_{in}, and I_{in} as functions of time for a transition from logic 1 to logic 0.

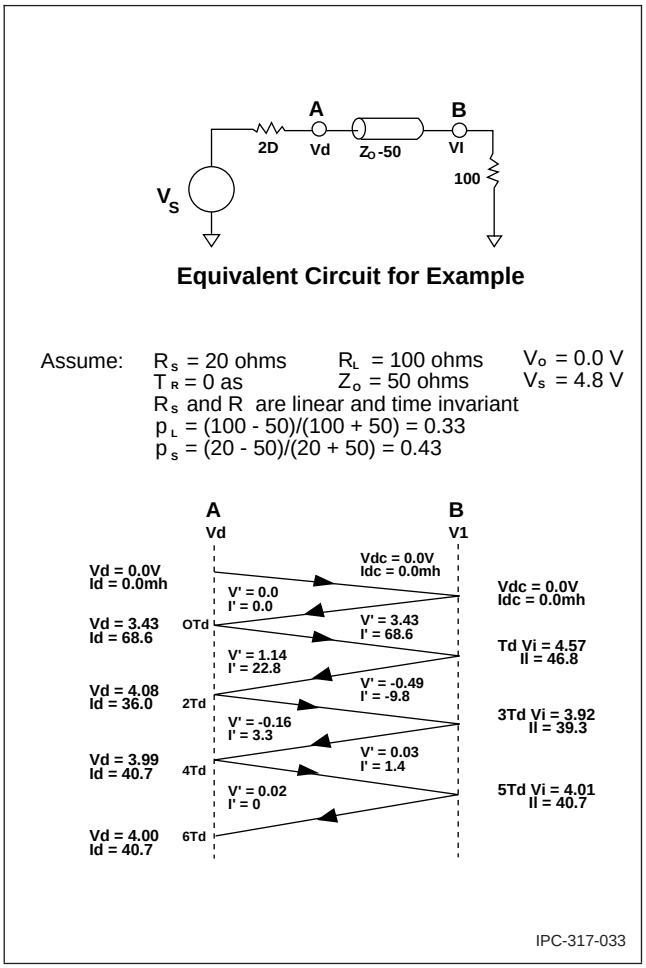


Figure 33 Equivalent circuit example

5.7 Crosstalk Due to the dense packaging and fast edge transitions of the selected logic families, noise due to crosstalk must be included in the signal AC noise budget. This section presents an in-depth model and formulas for determining the magnitude of crosstalk.

5.7.1 Model Noise caused by crosstalk is created by the coupling of adjacent signals from active lines to a passive line.

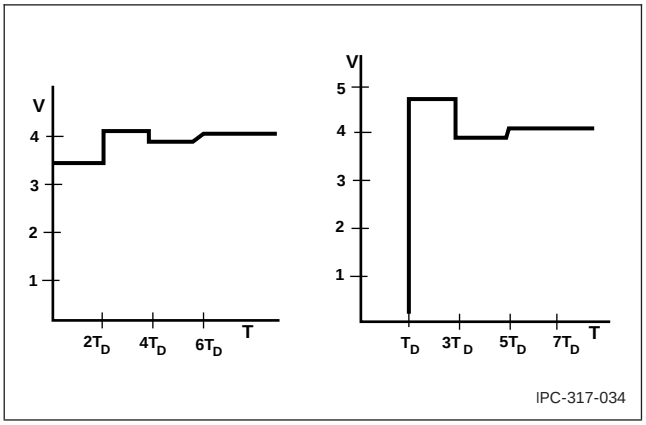


Figure 34 Predicted driver and load waveforms for Figure 57 a) Driver b) Load

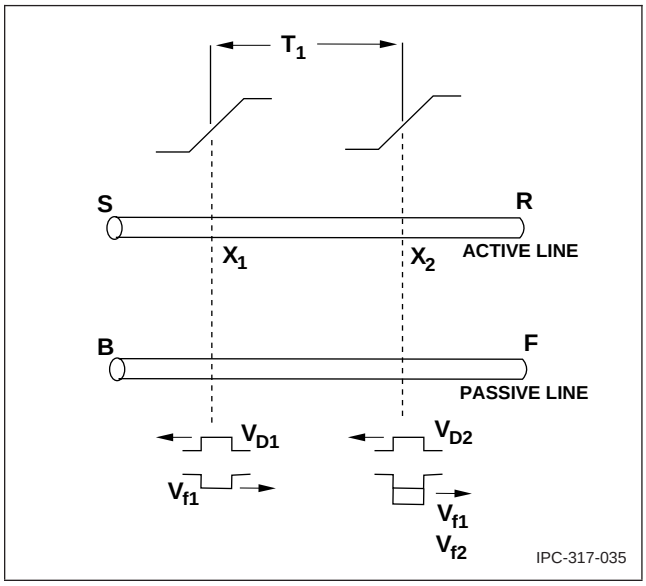


Figure 35 Induced crosstalk voltages

These lines are in close enough proximity as to create as appreciable mutual capacitance (C_M) and mutual inductance (L_M). The model of two lines in a crosstalk environment is illustrated in Figure 35. To cancel the effect of reflections in the model both lines are terminated to their characteristic impedance, Z_O. Both lines also have equal inherent propagation delays of T_D.

The following discussion references Figure 35. A pulse of magnitude V and edge transition rate ''a,'' (typically V/NS) is transmitted down the active line from point S. When it arrives at point X_1 currents are produced on the passive line due to mutual capacitance and inductance. Since the mutual capacitance sees equal capacitance either way on the passive line equal and opposite currents, I_C, are produced. Simultaneously, according to Lenz's Law, an equal but opposite inductive current, I_L, will be induced on the passive line.

At point B the currents, I_C and I_L, are additive and will produce a voltage of the same polarity as the active line. At point F the currents are opposite. Since the line is in a nonhomogenous environment I_C and I_L won't cancel. In general, I_L is greater than I_C. The summation of currents will, therefore, create a voltage of an opposite polarity than the active line at point F.

Assuming that $2 \bullet T_D > a$, the pulse on the active line will take T_D to propagate to point R at the end of the line. (Line length referred to here is the length of adjacency).

Consider the point in time that the pulse reaches X_1 of Figure 35. As was shown previously, two rectangular pulses which are proportional to the derivative of the active pulse will be created on the passive line. One pulse, V_{BL}, is a result of I_C plus I_L. It will propagate back towards point B. This will be the same polarity as the pulse on the active line.

A second pulse, V_{FL}, is a result of I_C minus I_L. It will be created and will propagate towards point F. This pulse will be opposite in polarity than the active pulse. After time T_L the

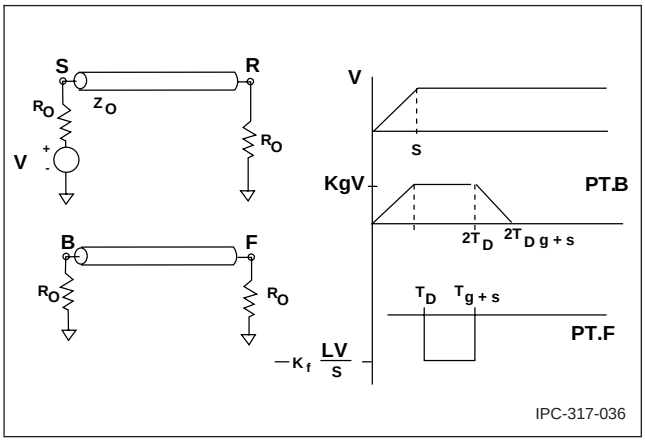


Figure 36 Crosstalk voltages for a line terminated at both ends

active pulse arrives at X_2. As before, the two pulses are created. During this time V_{FL} has propagated the same distance as the active pulse and will add onto V_{F_2}. As the active pulse travels down the rest of the active line all n of the V_{FN} pulses will add until the active pulse reaches the end of the line. This pulse is defined as FORWARD CROSSTALK. As can be seen, its magnitude is proportional to the amount of coupling at each point X_N (the coupling ratio is the forward crosstalk constant, K_F) and the length of the line. The width of the pulse will be equal to the risetime of the active pulse. The pulse that is the result of the addition of I_L and I_C that was created at point X_1 travels toward point B. When the active pulse arrives at X_2, T_1 time later, another identical pulse is created and also starts traveling towards point B. The pulse at X_1 will then be 2 • T_1 ahead of V_B. As the active pulse travels down its line a succession of pulses 2 • T_1 apart will be induced on the passive line propagating towards point B. Therefore, point B will see a series of pulses for a time 2 • T_D after the risetime ''a'' of the active pulse. The magnitude of the pulse will be independent of the line length but will be proportional to the amount of coupling which creates the BACKWARD CROSSTALK (the coupling ratio is the backward crosstalk constant, K_B).

If a >2 • T_1, the backward crosstalk will be attenuated by 2 • T_1/a. The forward crosstalk pulse will also be attenuated by 1/a. Figure 36 shows the expected forward and backward crosstalk pulses for a properly terminated line.

For a line length greater 2 • Td the forward and backward crosstalk coefficients, K_F and K_B are

$$K_F = V_F \bullet a / (V \bullet D) \qquad 5.67)$$

$$K_B = V_B / V_I \qquad 5.68)$$

where, V_F = Forward crosstalk voltage
V_I = Voltage switch on active line
a = Edge transition time
D = Length of coupled region
V_B = Backward crosstalk voltage

5.7.2 Microstrip Transmission Line The forward and backward crosstalk coefficients are related to the impedance of the signal lines and the mutual inductance and capacitance between them. Values for both can be derived from the following equations.

$$K_B = C_O \bullet Z_O \bullet (K_L + K_C)/(4 \bullet T_D) \qquad 5.69)$$

$$K_F = -0.5 \bullet C_O \bullet Z_O \bullet (K_L - K_C) \qquad 5.70)$$

$$K_L = 0.55 \bullet e^{[-(A2 \bullet S/H + B2 \bullet W/H)]} \qquad 5.71)$$

$$K_C = 0.55 \bullet e^{[-(Al \bullet S/H + B1 \bullet W/H)]} \qquad 5.72)$$

where,

$A1 = 1 + 0.25 \bullet \ell n[(\varepsilon_r+1)/2]$
$A2 = 1 + 0.25 \bullet \ell n[(\mu_r+1)/2]$
$B1 = 0.1 \bullet \sqrt{(\varepsilon_r+1)}$
$B2 = 0.1 \bullet \sqrt{(\mu_r+1)}$
S = Line spacing

To generate the maximum crosstalk values for the victim line some knowledge of the load configurations must be known. To determine the effect of the induced crosstalk pulses on the loads the AC noise immunity characteristics of the loads and the crosstalk noise budget allocation must be known.

5.7.3 Embedded Microstrip Transmission Line The crosstalk equations for an embedded microstripline are the same as for the microstripline with the difference of a modified relative permittivity. For a line length greater than 2 • T_D the forward and backward crosstalk is the same as equations 5.67 and 5.69 with A1 equal to equation 5.70.

$$A1 = 1 + 0.25 \bullet \ell n[(\varepsilon'_r + 1)/2] \qquad 5.73)$$

$$\varepsilon'_r = \varepsilon_r \bullet [1 - e^{(-1.55 \bullet H'/H)}] \text{ (from 5.18)} \qquad 5.74)$$

where, H′ = Distance from reference plane to the top of the dielectric

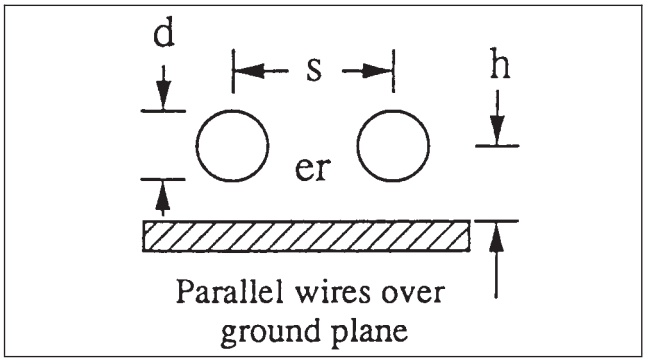
H = Distance from reference plane to the signal line

5.7.4 Backward Crosstalk Amplitudes

$$Vbx = \frac{k+1}{2} \cdot \frac{Zo}{2 \cdot Zm} \qquad a \le 2\tau \qquad 5.75a)$$

$$Vbx = \frac{k+1}{2} \cdot \frac{Zo}{2 \cdot Zm} \cdot \frac{2\tau}{a} \qquad a \ge 2\tau \qquad 5.75b)$$

$$Vfx = \frac{k-1}{2} \cdot \frac{Zo}{2 \cdot Zm} \cdot \frac{2\tau}{a} \qquad 5.75c)$$



where,

$$Zm = \frac{120}{\sqrt{er}} \cdot \frac{f1 \cdot f2}{f1 - f2} \quad 5.75d)$$

$$f1 = \ell n \cdot \left[\frac{4 \cdot h}{d}\sqrt{1+g^2}\right] \quad 5.75e)$$

$$f2 = \ell n \cdot \left[\frac{4 \cdot h}{g \cdot d} \cdot \frac{1}{\sqrt{1+\frac{1}{g^2}}}\right] \quad 5.75f)$$

$$g = \frac{2 \cdot h}{S} \quad 5.75g)$$

Variables

Zo = Characteristic impedance (in ohms)
Zm = Mutual impedance between lines (in ohms)
s = Wire spacing center to center (in mils)
er = Effective dielectric constant
d = Wire diameter (in mils)
h = Wire height − center to plane (in mils)
k = Constant to adjust for dielectric geometry (≈ 1.025)
a = Signal rise time (in nanoseconds)
Vbx = Backward crosstalk (Volts/V)
Vfx = Forward crosstalk (Volts/V)
τ = Parallel coupled region (in ns)
L = Parallel coupled length (in inches)

5.7.5 Stripline In the stripline environment the forward crosstalk equals zero. This is d0ue to K_L being equal to K_C. The back crosstalk will be twice the equivalent microstrip crosstalk (where the impedances are the same) because the capacitance is twice as high.

$$K_B = 2 \bullet V_B / V_I \quad 5.76a)$$

or,

K_B = equation 5.68

$K_F = 0$

Since the line is centered between the reference planes H is the distance from the signal line to either plane.

The crosstalk environment for the asymmetric line is the same as the stripline. Crosstalk between signal layers is negligible due to the orthogonality of the two layers.

5.7.6 TTL/MOS Models There are two configurations in which two lines with one driver and one receiver will have a common run. The first is with the drivers at the same end. The second is with the drivers at opposite ends.

Since the ''0'' state noise level is the most critical all the outputs and inputs common to the passive line used in the following analysis will be at this logic level. Figure 37 illustrates the condition with both drivers at the same end. Figure 38 illustrates the condition with the drivers at opposite ends.

When multiple lines are in parallel the noise coupled onto the passive line is additive but time synced. That is, if pulse on adjacent lines are next to the same location on the passive line at the same time, the resulting noise pulses will be directly additive.

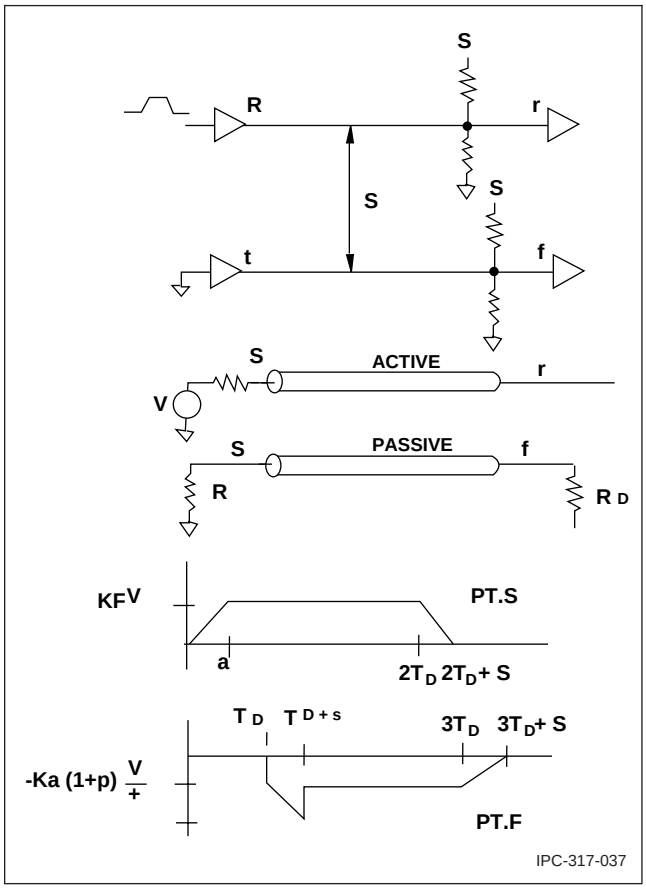


Figure 37 Drivers and receivers at a common end
a) Physical implementation
b) Model
c) Backward crosstalk
d) Forward crosstalk

The crosstalk pulse may have a relatively high amplitude and not cause any circuit problems. This is due to the inherent AC noise immunity of TTL devices. Figure 39 presents the AC noise immunity curves for some TTL logic families. These curves coupled with the fact that the noise pulse due to crosstalk will usually be narrower than the gate propagation delay will allow a large pulse at the input to the device, without affecting the contents or the output.

5.8 Signal Attenuation The two principal causes of signal attenuation are resistive losses due to the conductor, and dielectric losses. These two loss mechanisms will be discussed separately in the following two sections.

5.8.1 Resistive Losses (Skin Effect) For a conductor carrying an alternating electric current, the distribution of the current over the cross section of the conductor is nonuniform. The current density is greater at the surface of the conductor than at its center. This phenomenon, which is known as the skin effect, is due to electromagnetic (inductive) effects and becomes more pronounced as the frequency of the current is

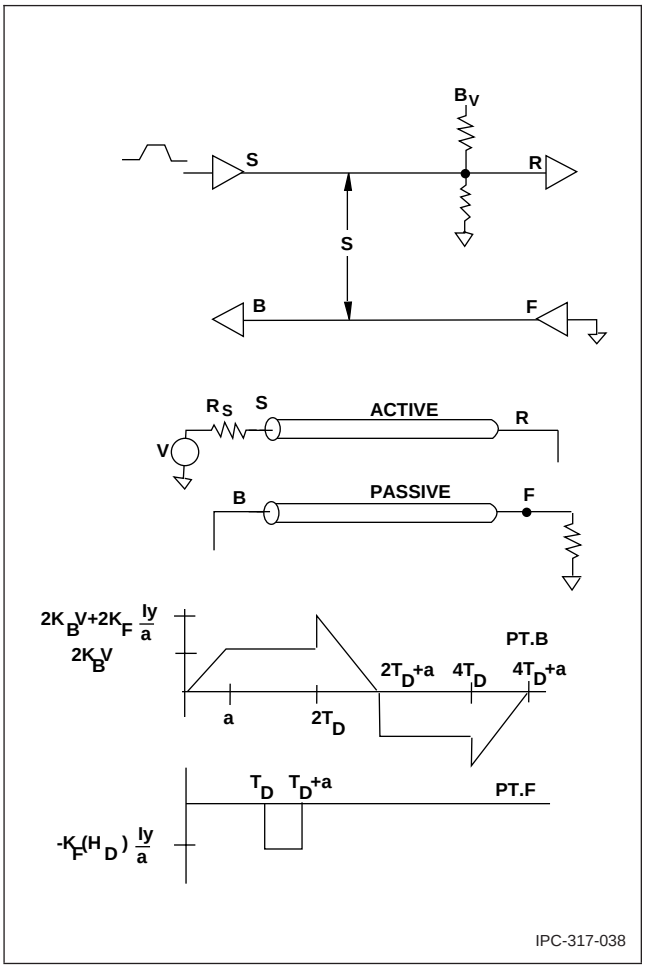


Figure 38 Drivers and receivers at opposite ends
a) Physical implementation
b) Model
c) Backward crosstalk
d) Forward crosstalk

increased. The distance, δ, at which the current density decays to 1/e of its value at the surface is called the skin depth, and may be obtained from the equation:

$$\delta = \frac{1}{\sqrt{\pi f \mu}} \qquad 5.76b)$$

where,

f is the frequency in Hz,
σ is the conductivity in mhos/m
μ is the absolute permeability of the conductor in H/m.

Thus, the effective resistance of a conductor carrying an alternating current is greater than the direct current resistance, and consequently, the power losses are greater than the usual I^2R, and rise proportionately with the square root of frequency. The effective surface resistivity, R_s, of a conductor is given by:

$$R_S = 1 / (\sigma\ \delta)\ [\text{ohms}] \qquad 5.77)$$

which on substitution for δ gives:

$$R_S = \left(\frac{\pi f \mu}{\sigma}\right)^{1/2} \qquad 5.78)$$

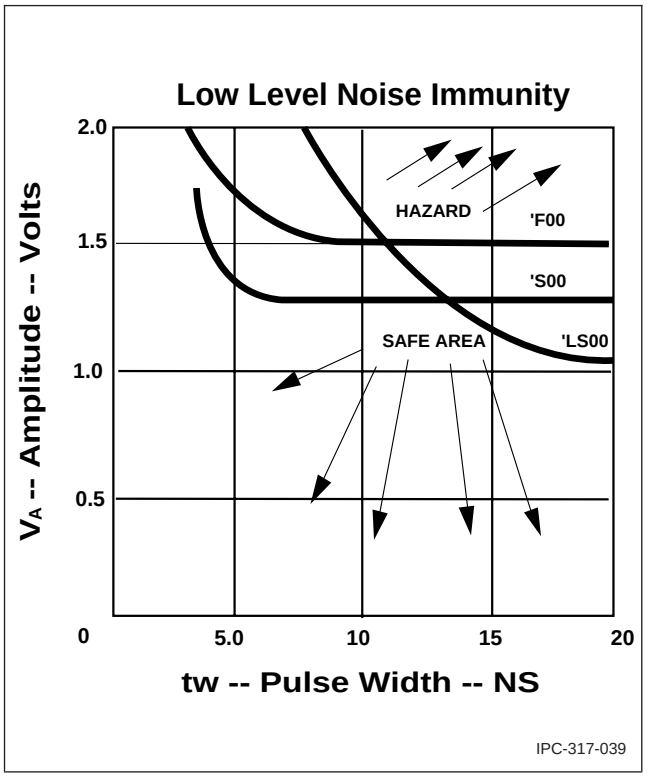


Figure 39 AC Noise immunity for selected TTL families

For copper, assuming a conductivity of σ = 5.8 x 10^7 mhos m^{-1} and its permeability to be that of free space (4π x 10^{-7} H m^{-1}), this leads to:

$$R_S = 2.61 \times 10^{-7} \sqrt{f}\ [\text{ohms}] \qquad 5.79)$$

The resistance, R, of a conductor of length, D, and circumference, C, is given by:

$$R = (D \bullet R_S) / C\ [\text{ohms}] \qquad 5.80)$$

This resistance may be used, with the usual I^2R relationship, to calculate the resistive power loss.

However, two cautionary notes must be added.

As a consequence of the micro roughness of the metal, the effective length of the conductor may be longer than its physical length, and the extent of the resistive power loss can be expected to vary with different conductor surface finishes. In addition, an assumption implicit in the above, is that the field lines extend uniformly from the conductor in all directions. This assumption is only completely accurate for a conductor of circular cross section, surrounded by a ground potential at infinity. For realistic circuit configurations, concentrations of field lines will be greater in some regions than in others, and this will lead to second order effects. For a more complete discussion of resistive losses for the stripline configuration the reader is referred to Howe (1974).

5.8.2 Dielectric Losses Energy is also absorbed by the dielectric medium surrounding the conductors. For the stripline configuration, signal attenuation by the dielectric is given

approximately by:

$$A_D = \frac{27.3 \tan \delta \sqrt{\varepsilon'_r}}{\lambda_0} \quad 5.81)$$

where,

λ_0 free space wave length
ε'_r effective relative permittivity and
tan δ loss tangent

Consequently, in order to minimize signal attenuation by the dielectric, it is desirable to select materials and the electrical configuration such that both ε'_r and tan δ are as low as possible. For other circuit configurations the above expression must be modified to replace tan δ with an effective tan δ'.

5.8.3 Rise Time Degradation Both of the principal mechanisms by which energy is absorbed from a propagating signal become more severe with increasing frequency; resistive losses are proportional to the square root of frequency, while the amount of energy absorbed by the dielectric medium is directly proportional to this quantity. Consequently, the higher the frequency of propagating signals the more closely losses and noise budgets should be examined.

In addition, for digital circuitry, this frequency dependence has ramifications upon the form in which pulse-shape corruption is manifested. A digital pulse may be represented by a sum of its Fourier components. Clearly, the higher frequency components of a transmitted pulse will be attenuated most rapidly. The highest frequency of concern, or bandwidth (BW) in Gigahertz, of a pulse of finite rise time, is given by:

$$BW = 0.35/T_R \text{ Ghz}$$

where, T_R in nanoseconds is the pulse rise time from 10% to 90% of its maximum value. Consequently, as the higher frequency components are absorbed, the bandwidth of the propagating pulse will decrease, producing a degradation of the rise time. Such rise time degradation is usually the most important effect of signal attenuation in digital circuits.

5.9 Computer Simulation Program The equations and techniques described in section 5 can be complex and difficult to solve manually. The following list of commercially available computer simulation programs may be used for high speed designs. Other programs are available. They will be included as the IPC is notified. (This list is not comprehensive, nor endorsed by the IPC.)

Company	Location	Software
Compact Software	Paterson, NJ	Supercompact
Deutsch Research	Palo Alto, CA	TurboSpice
EEsof, Inc.	West Lake Village, CA	jOmega, Libra, Touchstone
Hewlett-Packard Co.	Palo Alto, CA	Microwave Nonlinear Simulator
MetaSoftware Inc	Campbell, CA	HSpice
Micro Sim Inc	Irvine, CA	PSpice
Optotek Ltd.	Kanata, ON, Canada	MMICAD
Quad Design Technology Inc.	Camarillo, CA	XTK Crosstalk toolkit
Quantic Laboratories	Winnepeg, Man, Canada	Greenfield
Swiftlogic Inc.	Santa Clara, CA	Swiftline, Swiftnoise
Cadence	San Jose, CA	Analog Workbench
Cadence	Chelmsford, MA	DF/Sig Noise Analysis

5.10 Connectors

5.10.1 Sensitivity Connectors located within a conductive path are transparent to signals, a lumped element, provided that the signal bandwidth is not equivalent to, or less than the physical mated length of the connector. In digital switching systems, the rise time of the pulse, a gating factor, is used to determine the cutoff frequency (fo = 0.35/tr). Signal bandwidth is derived from the formula lambda = v/fo. The connector is ''lumped'' if the connector path length is <lambda/15 and ''distributed'' if the connector path is not. A distributed element must have transmission criteria applied to eliminate signal distortion.

5.10.2 Distributed Line Compensations Connectors found to be ''distributed,'' as described in section 5.10.1, should compensate the transmissability of their medium for ll or part of the following issues.

a. Impedance
b. Skew
c. Propagation delay (time)
d. Parasitic elements
e. Grounding
f. Crosstalk

The use of signal modeling software is suggested in order to ascertain the severity of impact on the overall circuit and the necessary compensating corrections.

5.10.3 Connector Types Connectors generally fall into the following electrical usage categories. The cutoff frequencies and bandwidths shown in the following table are generalizations of the category. Specific supplier parts will have their own unique values and tolerances owing to design and constructions (e.g. path length).

6.0 Performance Testing With the increase in importance of AC characteristics in the performance of circuit boards, fast and easy tests are needed to verify that the ''as built'' characteristics are within limits. Two of these characteristics are impedance and capacitance. In order to perform these tests, test structures must be built into test coupons on the outside of each circuit board directly into the circuit boards themselves. The test structures and test methods must be easy to use to insure fast, successful results when performed many

Connector Type	*Wavelength*	*Cutoff Frequency*
Isolated Pin	3 km	100KHz
Edge card (>.1 in grid)	30 m	10MHz
Open pin (.1 in & signal/gnd arrangement)	3 m	100 MHz
Reference plane	200 mm	1.5GHz
Coax	12 mm	25 GHz
Fiber Optics	30 um	10THz
Waveguide	1.5 um	200 THz

times at inspection. This section describes both of these topics and provides some suggested structures and equipment.

6.1 Impedance Testing The impedance of transmission lines in printed boards has an important effect on the high-speed performance of logic systems they contain. Impedance is expressed in ohms and is most often measured using Time Domain Reflectometers (TDRs).

6.1.1 Principle of Impedance Testing Using a TDR The principle on which TDRs operate is to send a very high-speed pulse (~200 picosecond rise time or faster) down the line being measured. At each change in impedance along the line, some of the energy from the pulse will be reflected back to the source end. A very high-speed sampling oscilloscope is attached at the source to display these reflections. The pulse source has a known output impedance, usually 50 ohms, that serves as the reference impedance. The amplitude of each reflection is proportional to the magnitude of the impedance change. The impedance of each segment of the line can be calculated from the percentage of the original pulse that is reflected back to the source.

Section 5.0 contains a detailed explanation of the reflection phenomenon and the calculations involved in deriving impedance. A more detailed explanation is contained in the operator's manual of each piece of TDR equipment. The operator is advised to read these document before measuring impedance.

6.1.2 Impedance Measuring Test Equipment Several models of TDR are available from suppliers of high-speed measuring equipment. Some are labeled cable testers, some are labeled simply TDRs, still others are labeled Impedance Test systems and include computers to perform all the calculations required to arrive at the impedance value for a given segment of a line.

6.2 Impedance Test Structures and Test Coupons

Impedance measurements can be performed on actual transmission lines in a circuit board or in conductors specially constructed to provide easy access to their ends. Because it is difficult to access the ends of transmission lines in most circuit boards, the specially built lines make impedance testing more convenient and reliable.

6.2.1 Test Structure Design The specially constructed impedance test lines may be designed into the body of the circuit board or into a test coupon designed for this purpose. In either case, the test line must be provided with a terminal at its end to which the test probe is attached. Close by, (0.1″ away or with a SMA connector, 0.14″ away) an AC ground contact must be provided to insure a good AC return for the test pulses. The length of each test line should be comparable in length to the signal lines with 6″ being a minimum. In order to insure the impedance tests accurately reflect the characteristics of the signal lines, the width and the electrical environment of the test line(s) must be the same as the signal lines and there must be a test line in each signal layer.

It is only necessary to provide contact to one end of a test line in order to make an impedance measurement. However, if contacts are provided at each end a wider assortment of testers and test methods can be employed. Since the area cost of an additional contact point and its associated ground contact is minimal, it is advisable to provide test contacts at both ends of each test line.

6.2.2 Test Probes and Connections Some impedance tests call for connecting subminiature connectors to the line ends. This is not economical in most digital logic boards nor is it necessary. It is possible to connect test probes to the end of the TDR cables that consist of two contacts 0.1″ apart or with a SMA connector, 0.14″ apart. This type of contact is economical and provides rapid contact to the test structures. Because it is a small structure, it does not introduce discontinuities that materially affect the impedance tests.

6.2.3 Locating Impedance Test Structures As high performance logic circuit boards grow larger and more complex, the complexity of the impedance test structures grow with them. As a result, building these structures into a test coupon becomes less practical. In addition, real estate may not be available in the fabricator's economical panel size in which to build a test coupon. If this occurs, the test coupon may substantially increase the cost of the finished circuit board.

6.2.3.1 Building Test Conductors Into the Printed Board Designing test conductors into a circuit board involves routing conductors on signal layers in areas not being used by the actual logic connections. In almost all cases, this can be done without penalty. In this way, horizontal test conductors will be built into horizontal layers and vertical test conductors into vertical layers.

An advantage of building the test conductors into the body of the circuit board is that the test structures are carried along with the circuit board eliminating the need to provide tracking of test coupons.

6.2.3.2 Designing an Impedance Test Coupon Designing an impedance test coupon involves creating a long, narrow circuit board that is attached to the circuit board to be evaluated along one edge. The attachment point must be small to facilitate easy removal. The test coupon must contain all of the signal and power layers contained in the circuit board. The

board should be conditioned with respect to the typical operating temperature of the circuit board being designed. Test lines must be built into each layer as described above. Some provision should be made to ensure traceability between the coupon and the circuit boards.

6.2.4 A Simple Impedance Test Method The impedance of a transmission line can be determined by terminating its far end in a terminating resistor of a value that absorbs all of the incident signal, producing no reflection (see Figure 41). A straight forward way to do this is to attach the TDR as is done for any impedance test, setting it up so that the reflection from the open line end is at midscreen. Attach a miniature single-turn noninductive trimpot to the far end of the line between the end and ground. Slowly adjust the trimpot until the line on the display is flat between the line and beyond (no reflection). This is the condition of ideal/perfect termination. Measuring the resistance value of the trimpot with a digital mult-meter (DMM) establishes the impedance of the line under test.

This method is offered because it is quick, accurate and can be done repeatedly without requiring accurate calibration of the equipment and without requiring complex calculations or a computer.

6.3 Stripline Impedance Test Coupon The test coupon below (Figure 40) provides a stripline transmission line coupon for each signal layer of the circuit board. The coupon provides a mounting pattern for a standard SMA/SMC board connector with a 0.035 inch center pin hole. A TDR can be connected to either end for the impedance measurement.

The test trace can be on an attached coupon or be a trace on the circuit board.

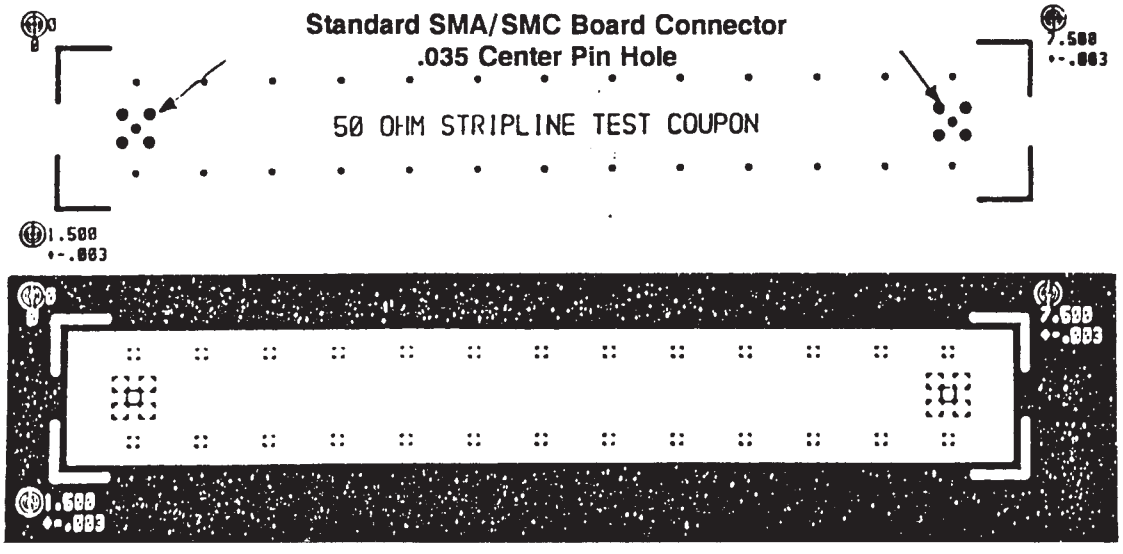


Figure 40

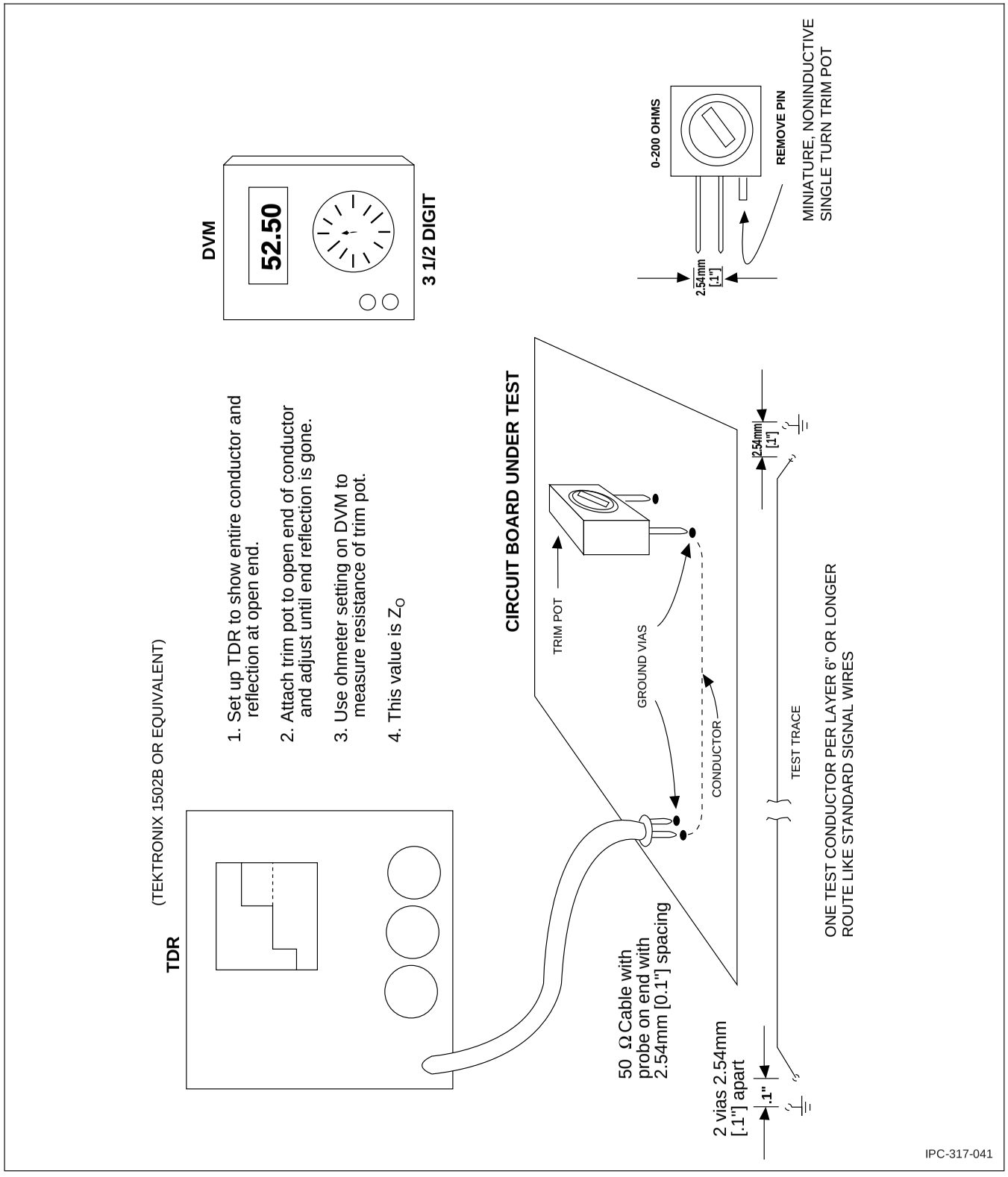


Figure 41 Test setup for measuring conductor impedance (suitable for receiving inspection)

Appendix A

DEVICE CHARACTERISTICS

This appendix presents summary tables and graphs that can be used in established digital device high speed performance characteristics. These data are typical and should be used as such.

A.1 74Fxxx Fairchild Advanced Schottky TTL (FAST) is faster, dissipates less power, has a higher more tightly controlled threshold voltage, lower input current, higher output current, and lower input and output capacitance than Schottky TTL. These are bipolar devices packaged in DIP and SM packages.

A.1.1 74Fxxx DC Characteristics

Table A.1 74Fxxx Family Characteristics

	Parameter	Value	Units
VIM	MIN Input HIGH Voltage	2.0	Volts
VIL	MAX Input LOW Voltage	0.8	Volts
VOH	MIN Output HIGH Voltage	2.7	Volts
VOL	MAX Output LOW Voltage	0.5	Volts
IOH	MAX Output HIGH Current	–1.0	mA
IOL	MAX Output LOW Current	20	mA
IIH	MAX Input HIGH Current	20	uA
IIL	MAX Input LOW Current	–0.6	mA
IOZH	MAX 3S HIGH OFF Current	50	uA
IOZL	MAX 3S LOW OFF Current	–50	uA
IOS	MAX Output Short Current	–150	mA
KyHL	HL Capacitive Drive	0.03	ns/pf
KyLH	LH Capacitive Drive	0.03	ns/pf
ICCL	Supply Current, LOW	2.55	mA
ICCH	Supply Current, HIGH	0.70	mA
TpLH	LH Propagation Time	3.9	ns (ρ 15 pf)
TpHL	HL Propagation Time	3.6	ns (ρ 15 pf)
NMH	Noise Margin HIGH	700	mV
NML	Noise Margin LOW	300	mV
FOH	Fanout HIGH	50	
FOL	Fanout LOW	33	
Tr	10– 90% Rise Time (Typ)	1.2	nS
Tf	90– 10% Fall Time (Typ)	1.2	nS
Zom	Line Impedance MIN	35	ohms
C1	Max Input Capacitance	4.0	pf

The typical data presented above is for Vcc = 5.0V ±5% and Ta = 0 to 70°C.

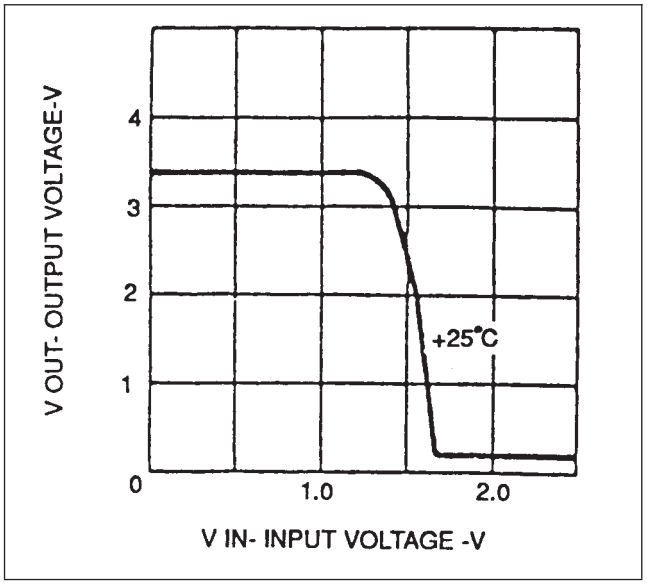


Figure A.1 74Fxxx V_O vs. V_i

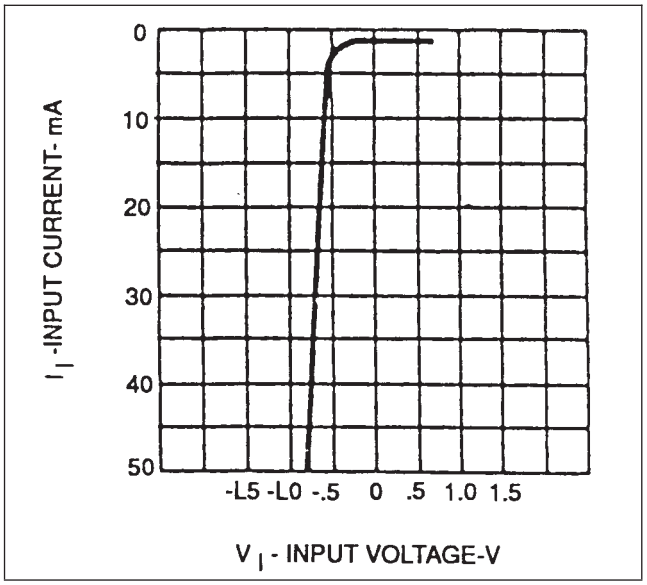


Figure A.2 74Fxxx I_O vs. I_i

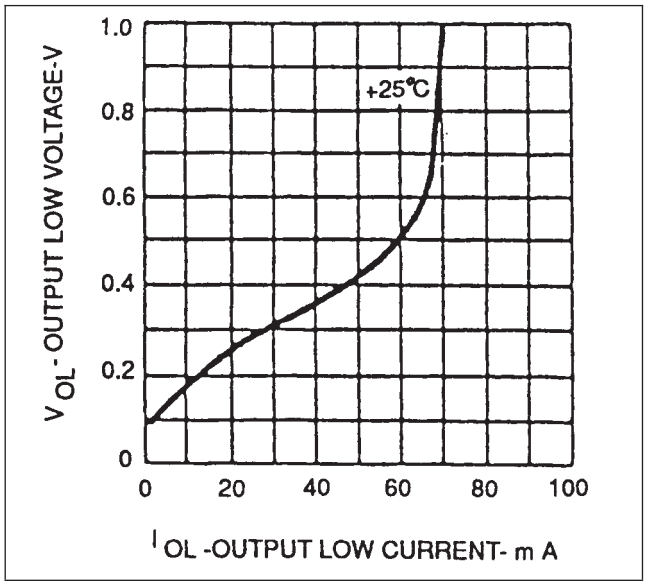


Figure A.3 74Fxxx V_{ol} vs. I_{ol}

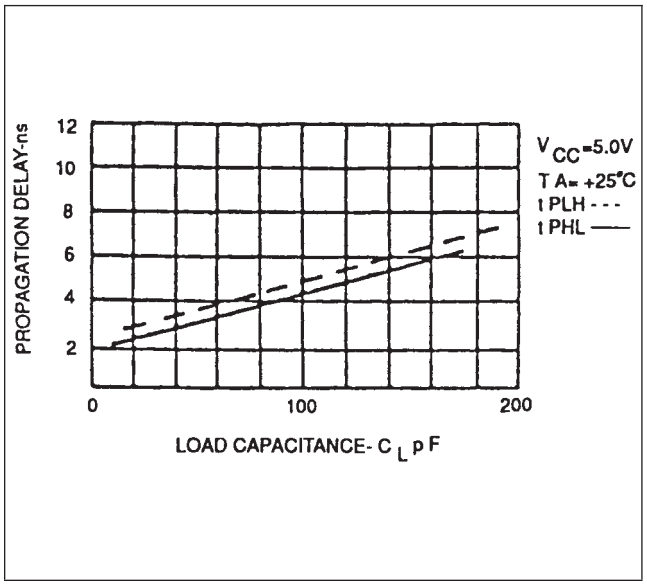


Figure A.5 74Fxxx Propagation Delay vs. Load Capacitance

A.1.2 74Fxxx AC Characteristics

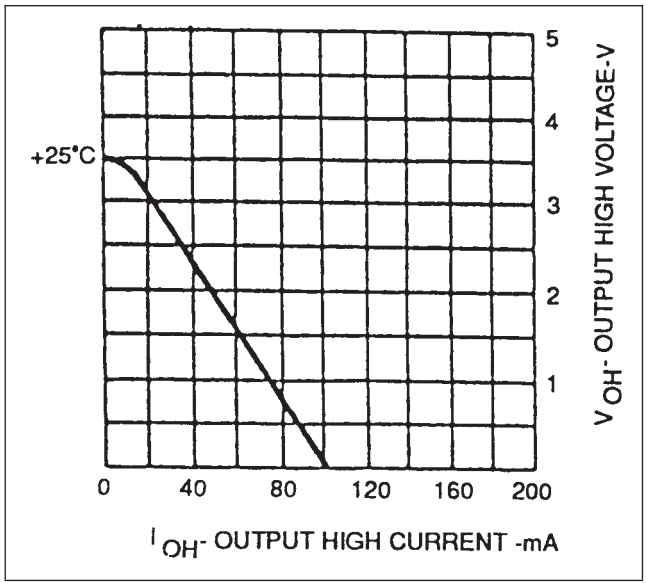


Figure A.4 74Fxxx V_{oh} vs. I_{oh}

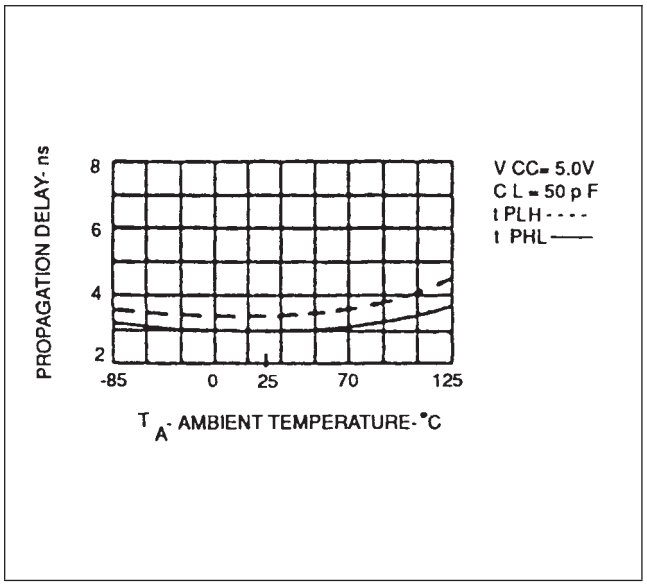


Figure A.6 74Fxxx Propagation Delay vs. Temperature

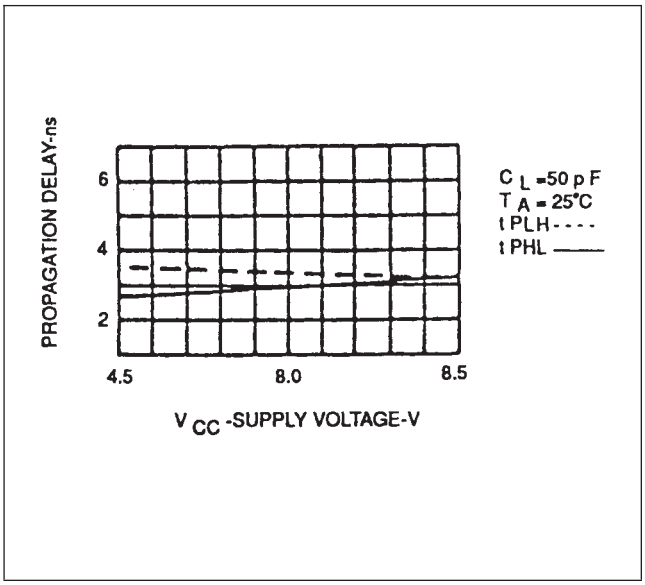


Figure A.7 74Fxxx Propagation Delay vs. Vcc

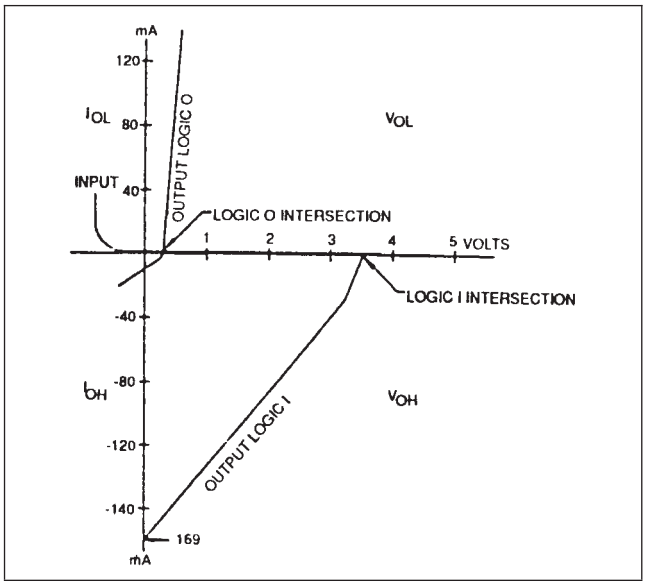


Figure A.9 74F24x Bergeron Plot

A.1.3 74Fxxx Power Dissipation

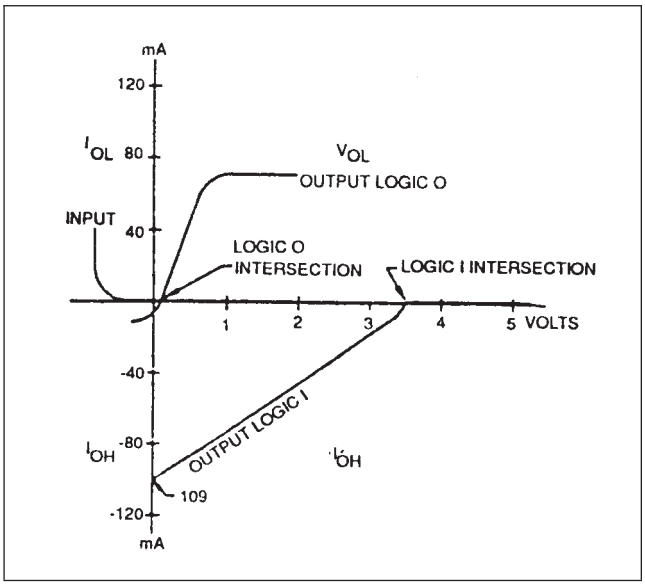


Figure A.8 74Fxxx Bergeron Plot

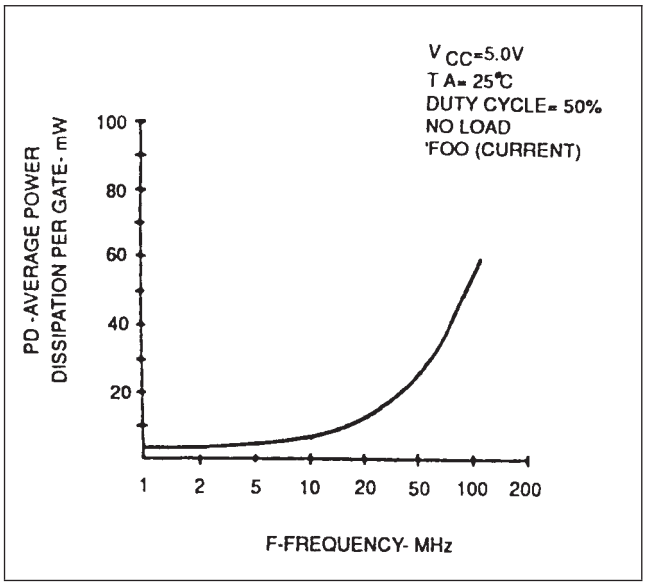


Figure A.10 74Fxxx Dissipation vs. Frequency

A.2 74Sxxx Schottky TTL is faster, dissipates more power than 74Fxxx. These are bipolar devices packaged in DIP and SM packages.

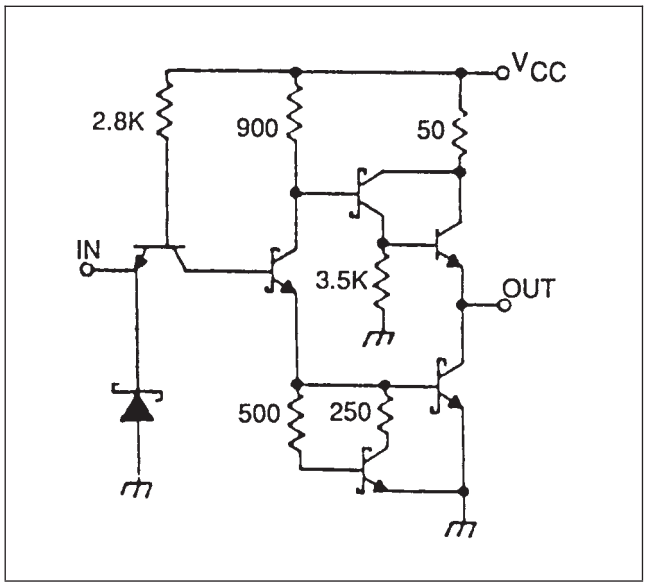


Figure A.11 Schottky TTL Inverter Structure

A.2.1 74Sxxx DC Characteristics

The typical data presented in Table A.2 is for Vcc = 5.0V ±5% and Ta = 0 to 70°C.

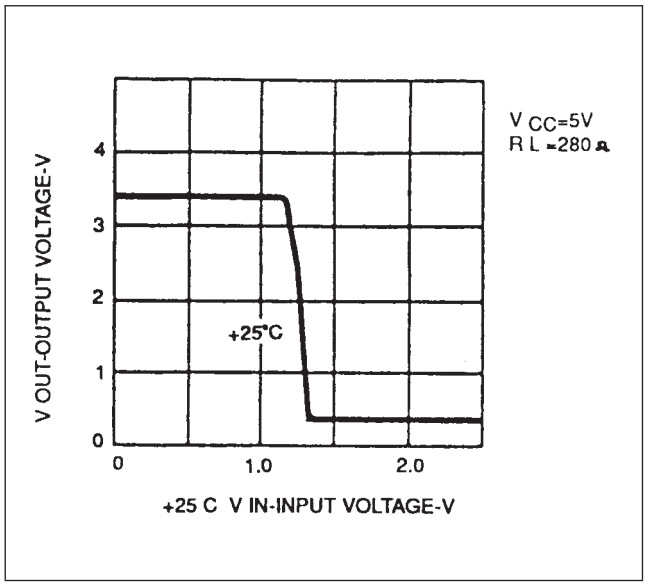


Figure A.12 74Sxxx V_o vs V_i

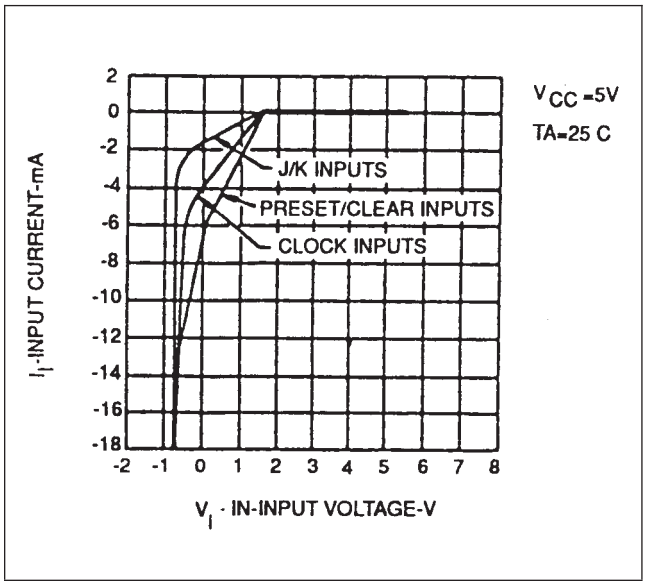


Figure A.13 74Sxxx V_i vs.I_i

Table A.2 74Sxxx Family Characteristics

	Parameter	*Value*	*Units*
VIM	MIN Input HIGH Voltage	2.0	Volts
VIL	MAX Input LOW Voltage	0.8	Volts
VOH	MIN Output HIGH Voltage	2.7	Volts
VOL	MAX Output LOW Voltage	0.5	Volts
IOH	MAX Output HIGH Current	–1.0	mA
IOL	MAX Output LOW Current	20	mA
IIH	MAX Input HIGH Current	50	uA
IIL	MAX Input LOW Current	–2.0	mA
IOZH	MAX 3S HIGH OFF Current	50	uA
IOZL	MAX 3S LOW OFF Current	–50	uA
IOS	MAX Output Short Current	–100	mA
KyHL	HL Capacitive Drive	0.03	ns/pf
KyLH	LH Capacitive Drive	0.05	ns/pf
ICCL	Supply Current, LOW	9.0	mA
ICCH	Supply Current, HIGH	4.0	mA
TpLH	LH Propagation Time	4.5	ns (ρ 15 pf)
TpHL	HL Propagation Time	5.0	ns (ρ 15 pf)
NMH	Noise Margin HIGH	700	mV
NML	Noise Margin LOW	300	mV
FOH	Fanout HIGH	20	
FOL	Fanout LOW	10	
Tr	10– 90% Rise Time (Typ)	3.5	nS
Tf	90– 10% Fall Time (Typ)	2.0	nS
Zom	Line Impedance MIN	50	ohms
C1	Max Input Capacitance	5.0	pf

A.2.2 74Sxxx AC Characteristics

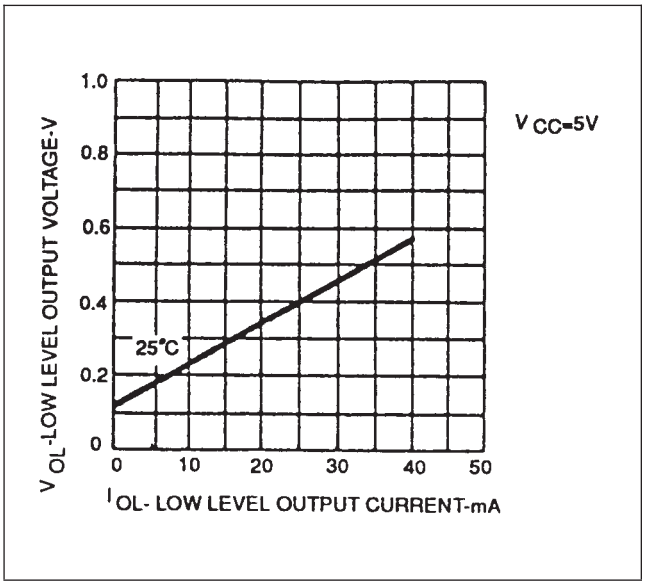


Figure A.14 74Sxxx V_{ol} vs. I_{ol}

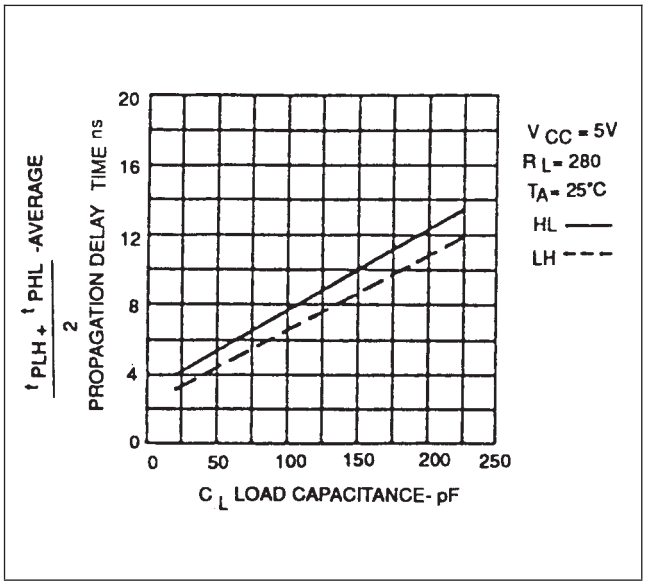


Figure A.16 74Sxxx Propagation Delay vs. Load Capacitance

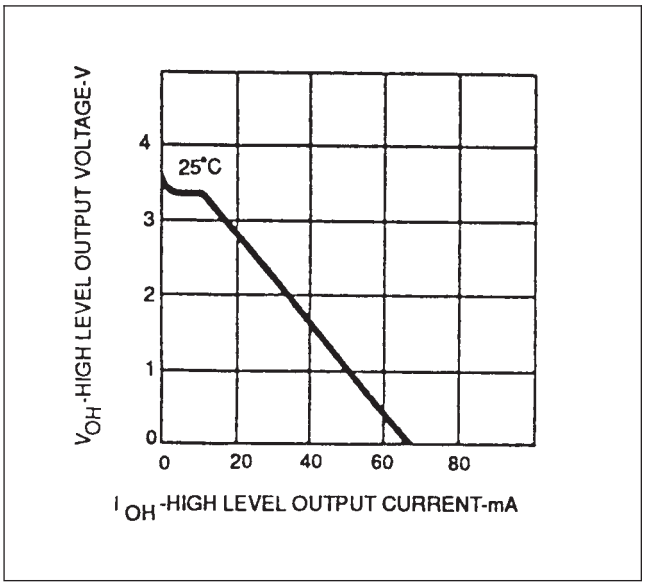


Figure A.15 74Sxxx V_{oh} vs. I_{oh}

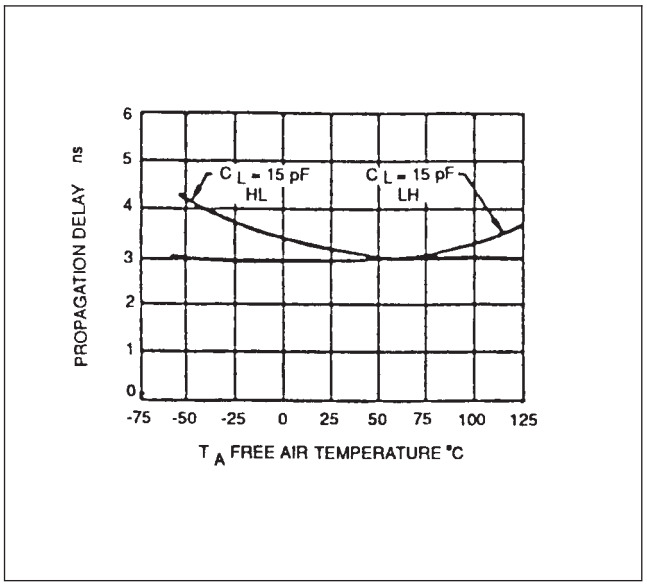


Figure A.17 74Sxxx Propagation Delay vs. Temperature

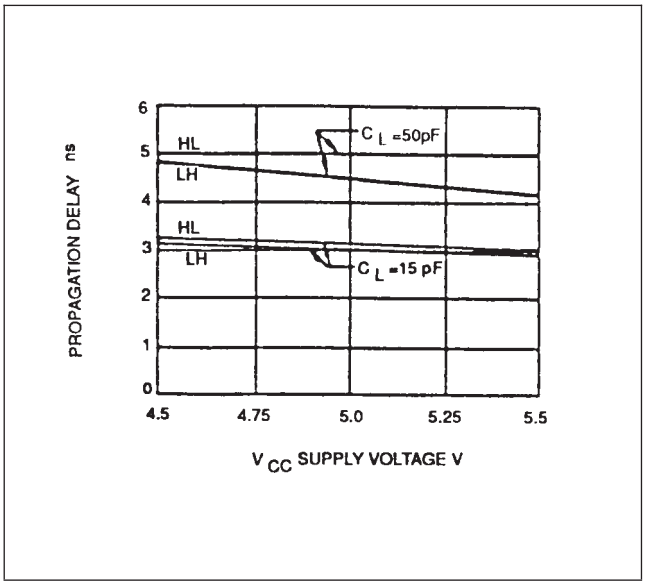


Figure A.18 74Sxxx Propagation Delay vs. Vcc

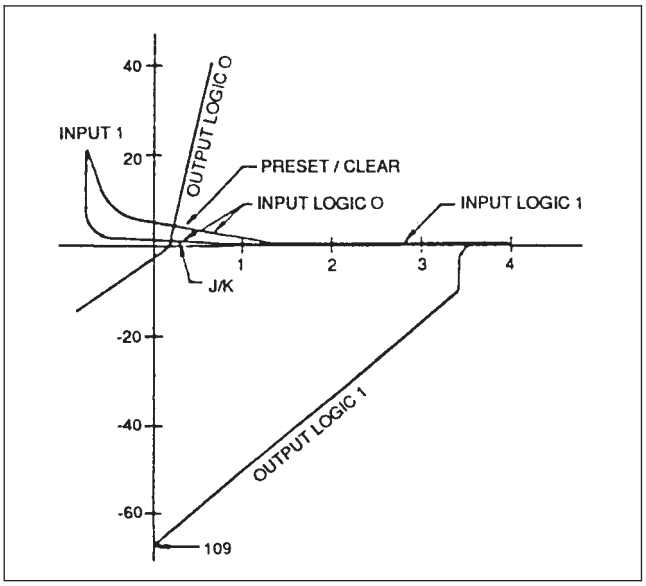


Figure A.19 74Sxxx Bergeron Plot

A.2.3 74Sxxx Power Dissipation

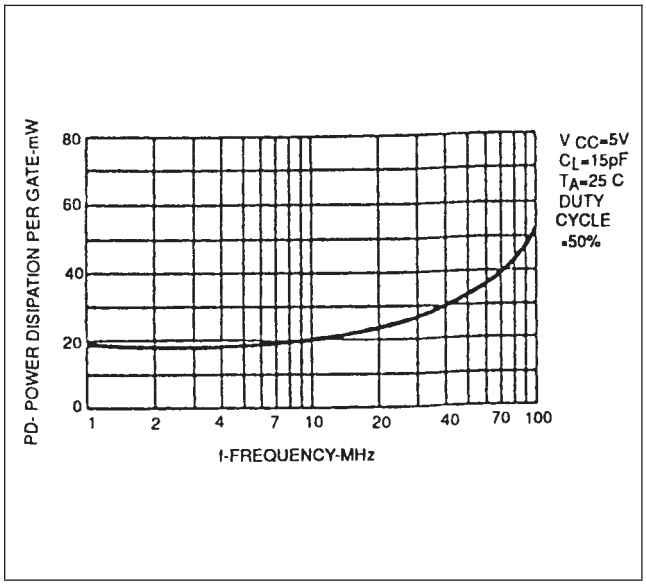


Figure A.20 74Sxxx Power Dissipation vs. Frequency

A.3 74ASxxx Advanced Schottky TTL (AS) is faster, dissipates more power, has a higher, more tightly controlled threshold voltage, lower input current, higher output current and lower input and output capacitance than Schottky TTL. These are bipolar devices packaged in DIP and SM packages.

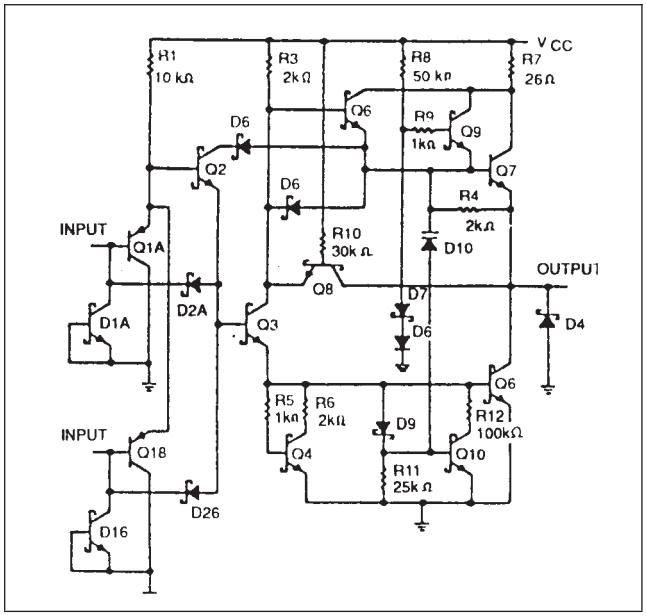


Figure A.21 AS Inverter Structure

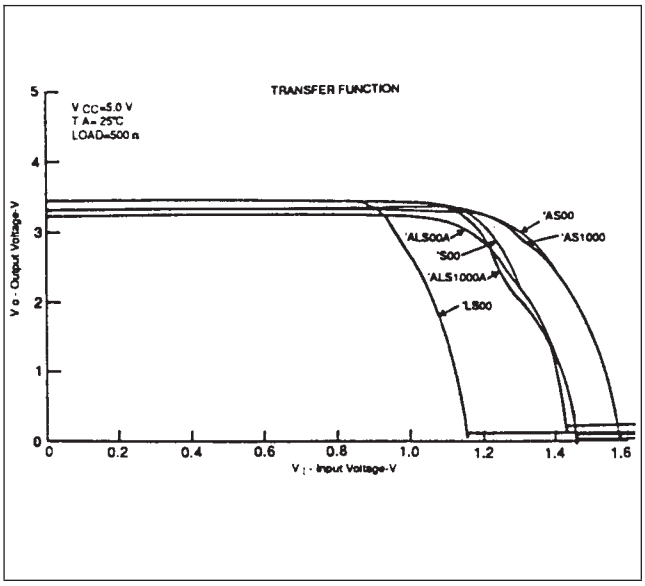


Figure A.22 74ASxxx V_o vs. V_i

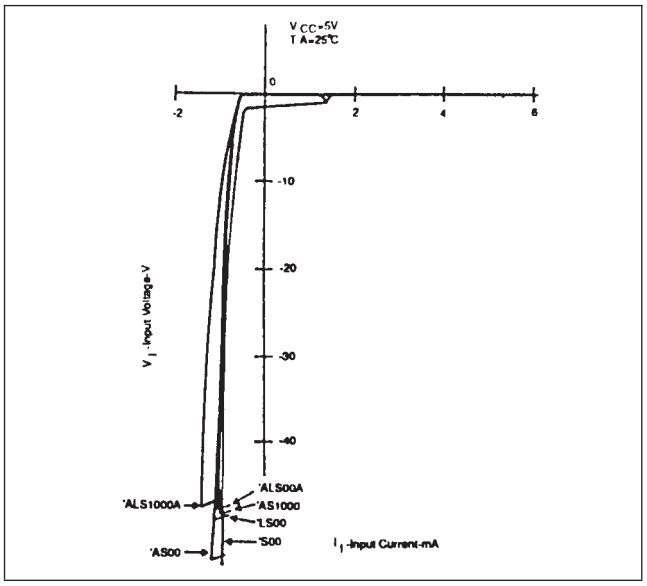


Figure A.23 74ASxxx V_i vs. I_i

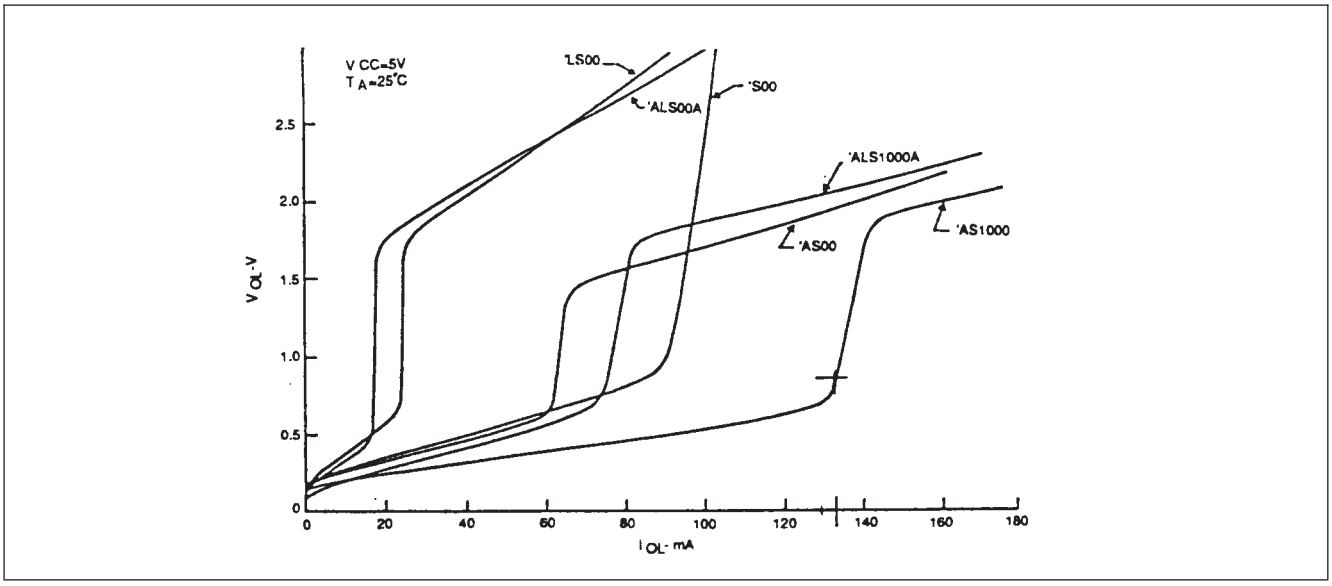


Figure A.24 74ASxxx V_{ol} vs. I_{ol}

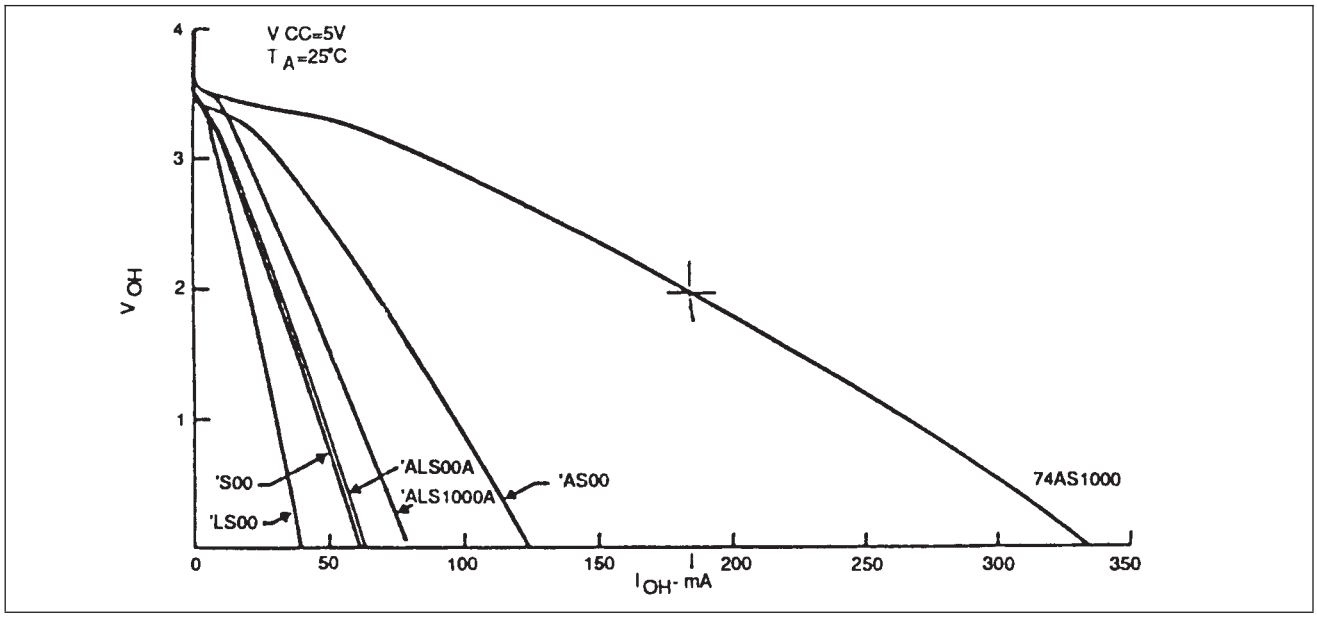


Figure A.25 74ASxxx V_{oh} vs. I_{oh}

A.3.2 74ASxxx AC Characteristics

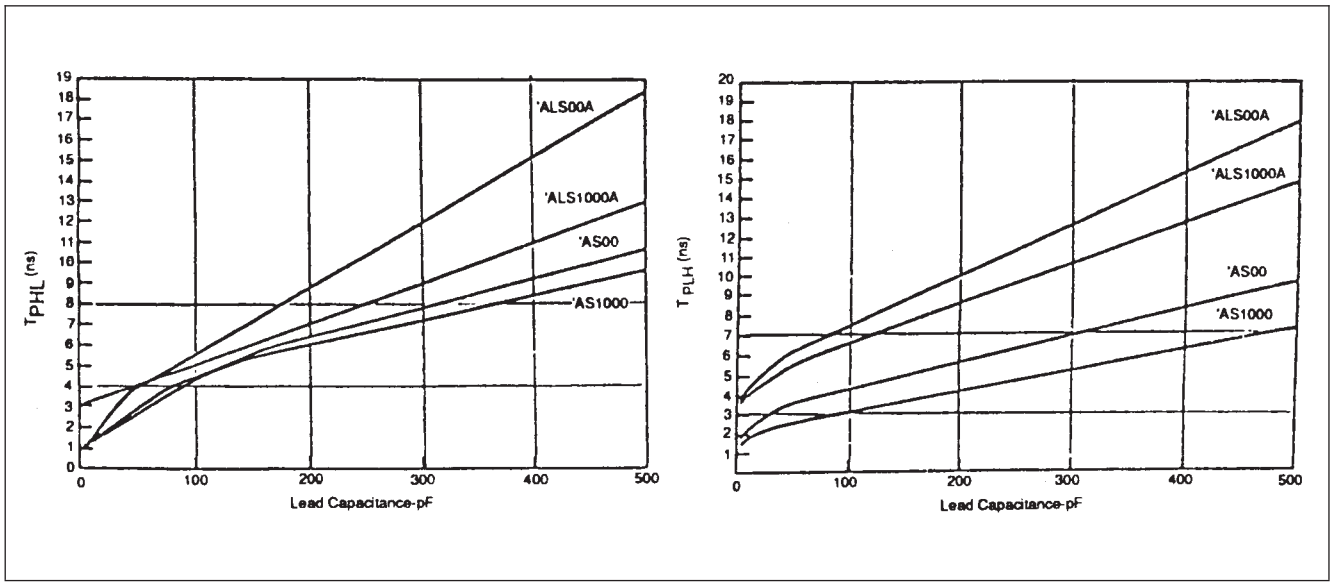


Figure A.26 74ASxxx Propagation Delay vs. Load Capacitance

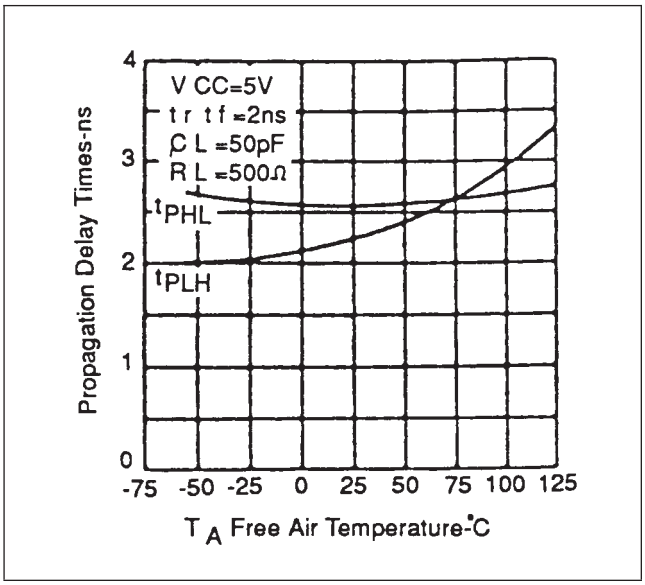


Figure A.27 74ASxxx Propagation Delay vs. Temperature

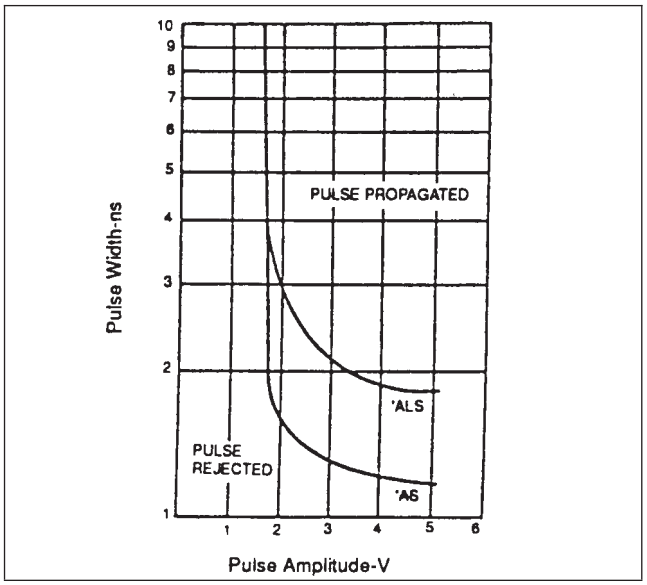


Figure A.29 74ASxxx Noise Immunity

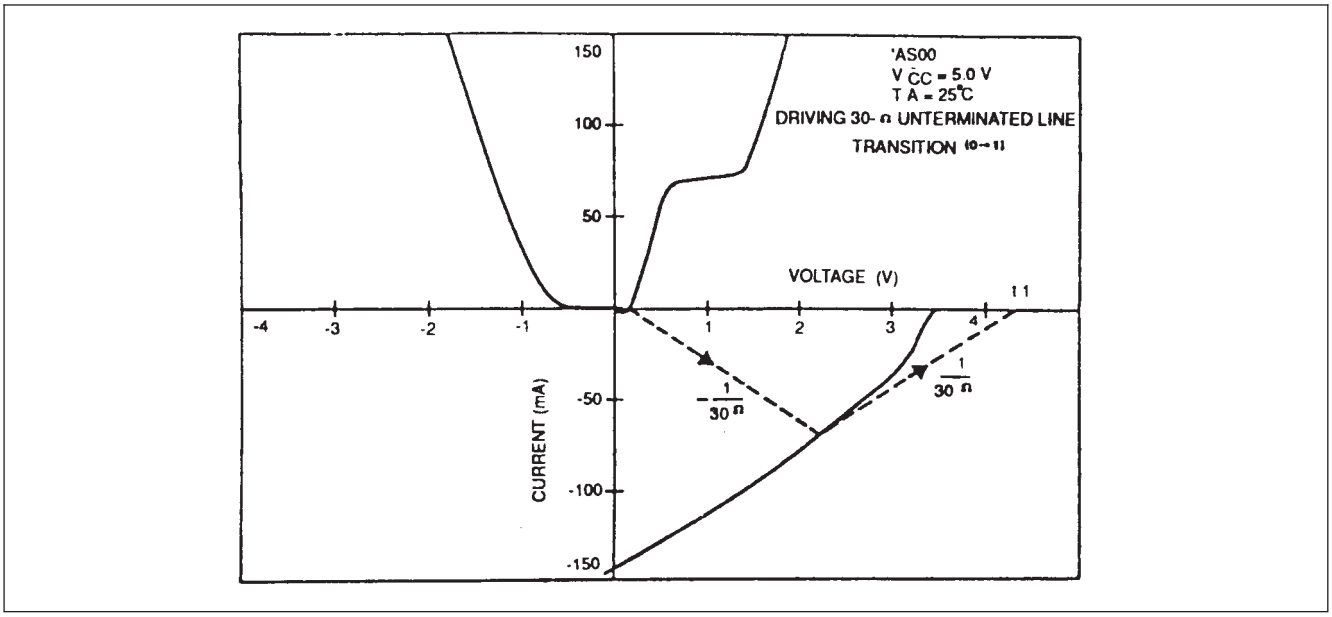


Figure A.28 74ASxxx Bergeron Plot

A.3.3 74ASxxx Power Dissipation

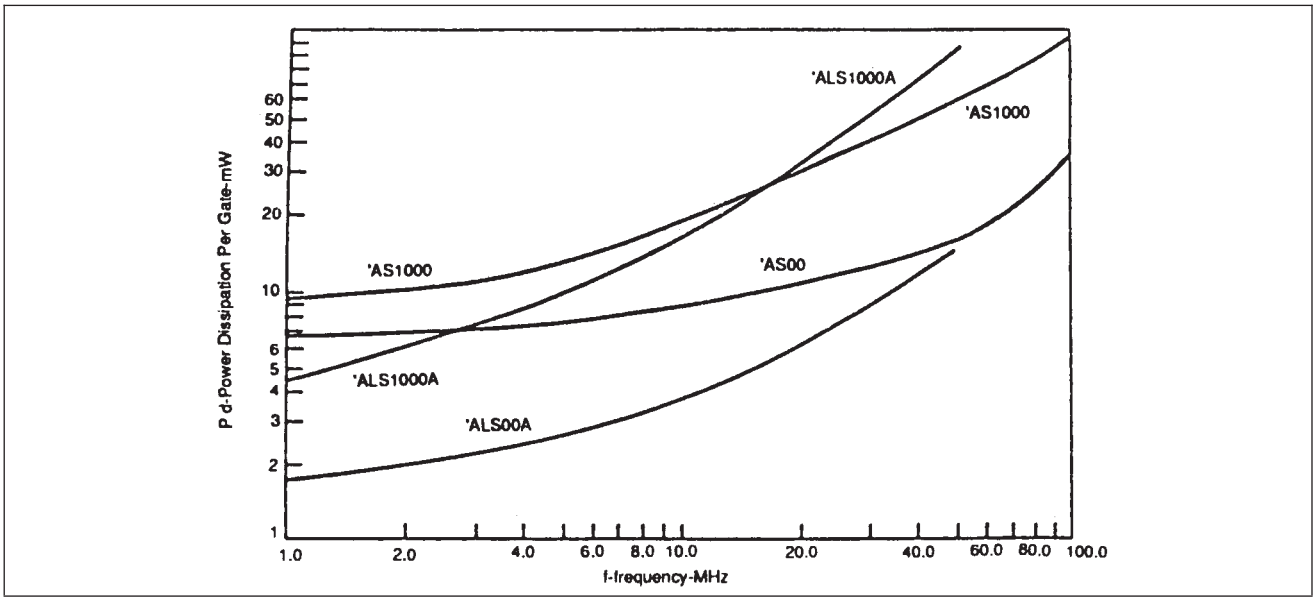


Figure A.30 74ASxxx Power Dissipation vs. Frequency

A.4 74LSxxx Low power Schottky TTL (LS) is slowerfaster, dissipates less power than 74Sxxx. These are bipolar devices packaged in DIP and SM packages.

A.4.1 74LSxxx DC Characteristics

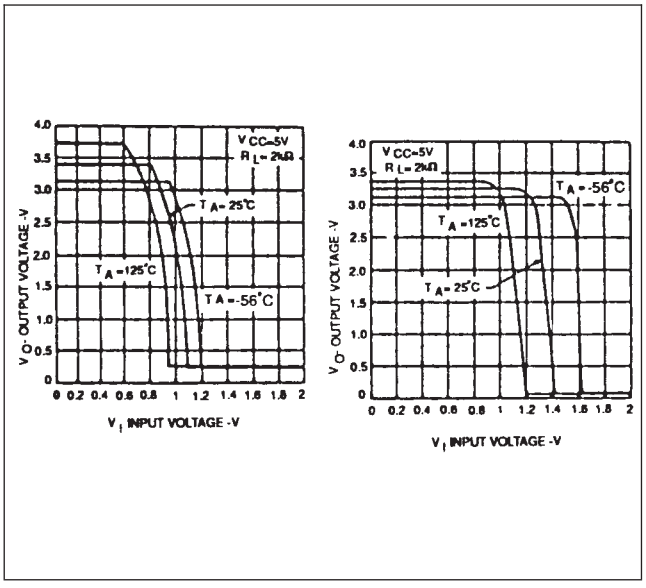


Figure A.31 74LSxxx V_o vs. V_i

A.4.2 74LSxxx AC Characteristics

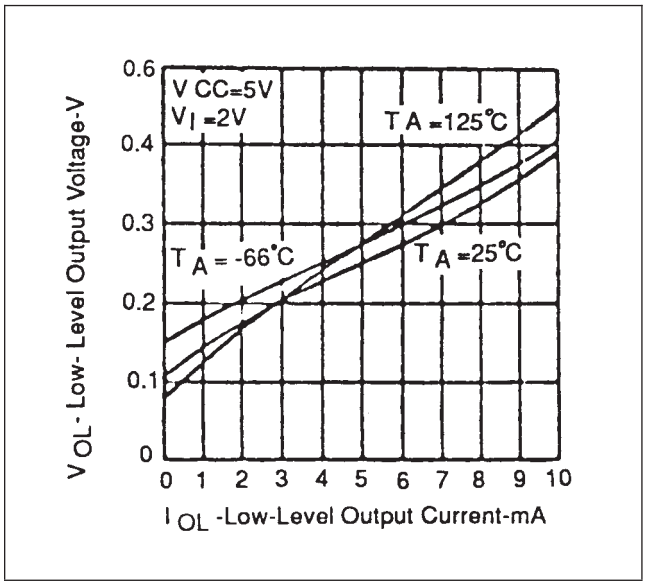


Figure A.32 74LSxxx V_{ol} vs. I_{ol}

A.4.2 74LSxxx AC Characteristics

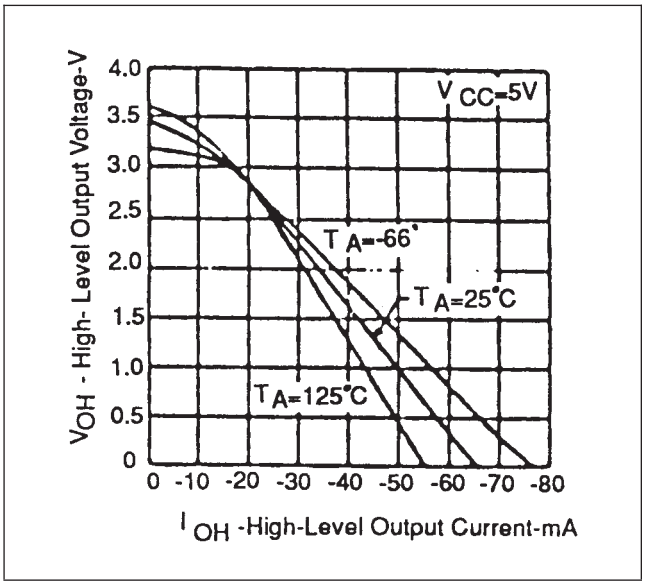


Figure A.33 74LSxxx V_{oh} vs. I_{oh}

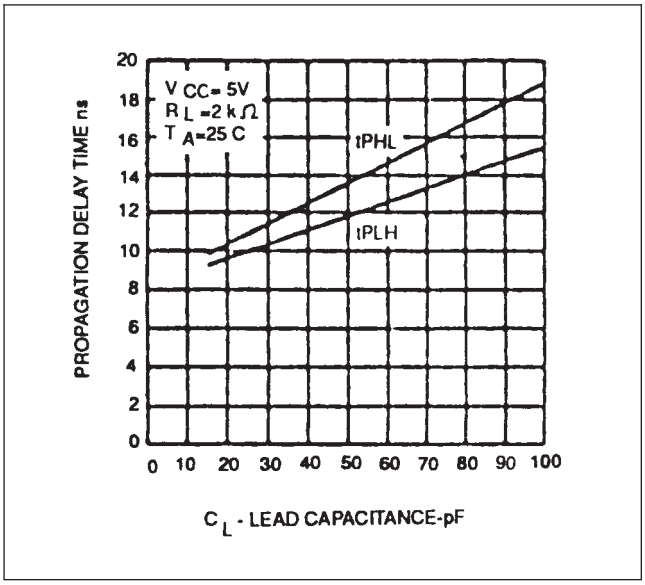


Figure A.34 74LSxxx Propagation Delay vs. Load Capacitance

A.4.3 74LSxxx Power Dissipation

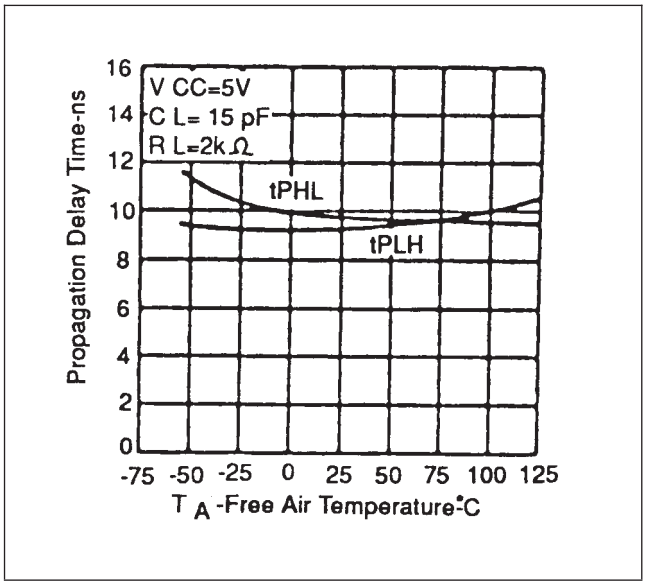


Figure A.35 74LSxxx Propagation Delay vs. Temperature

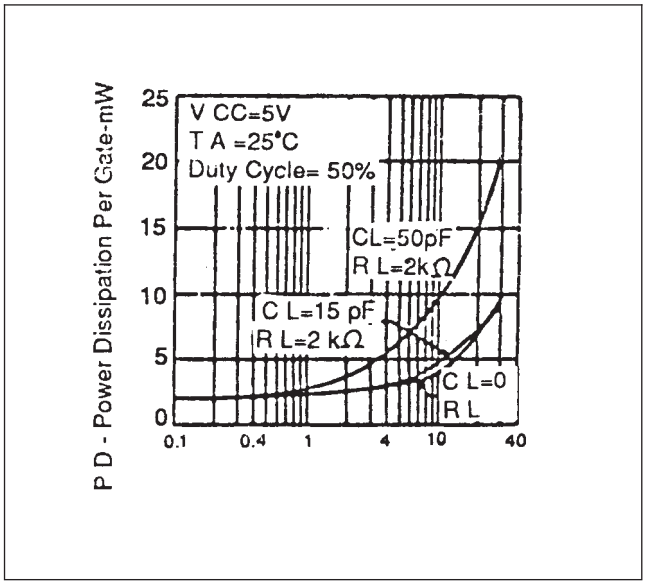


Figure A.36 74LSxxx Power Dissipation vs. Frequency

A.5 74ALSxxx Advanced Low Power Schottky TTL (ALS) is faster, dissipates less power, and lower input and output capacitance than Low Power Schottky TTL. These are bipolar devices packaged in DIP and SM packages.

A.5.1 74ALSxxx DC Characteristics

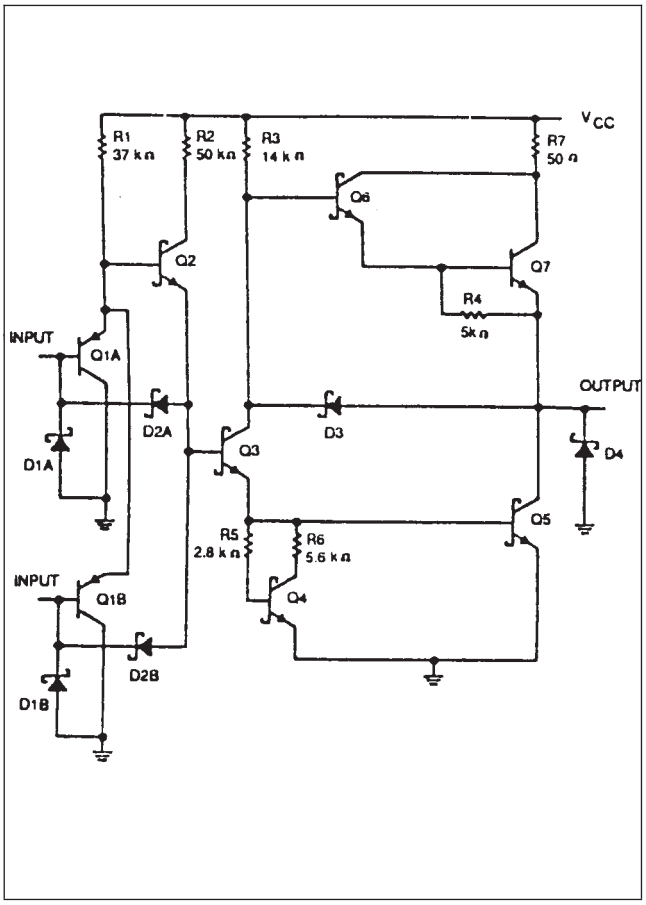


Table A.3 74ALSxxx Family Characteristics

The typical data presented above is for the Vcc = 5.0 V ± 5% and Ta = 0 to 70 °C.

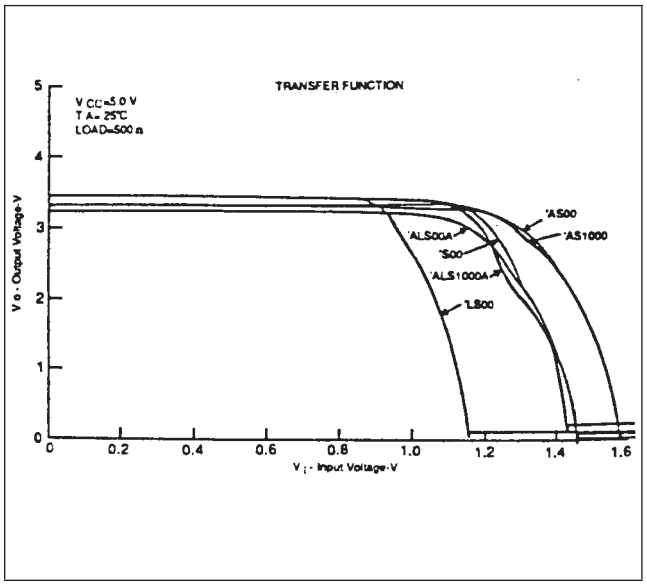


Figure A.37 74ALSxxx V_o vs. V_i

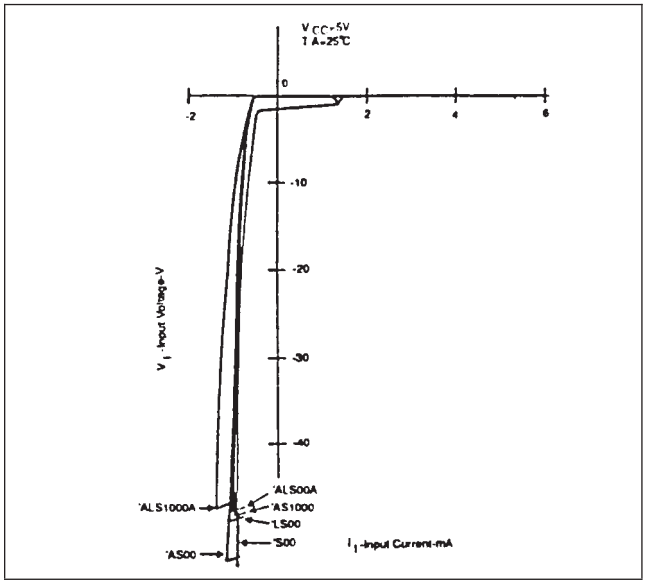


Figure A.38 74ALSxxx V_{in} vs. I_i

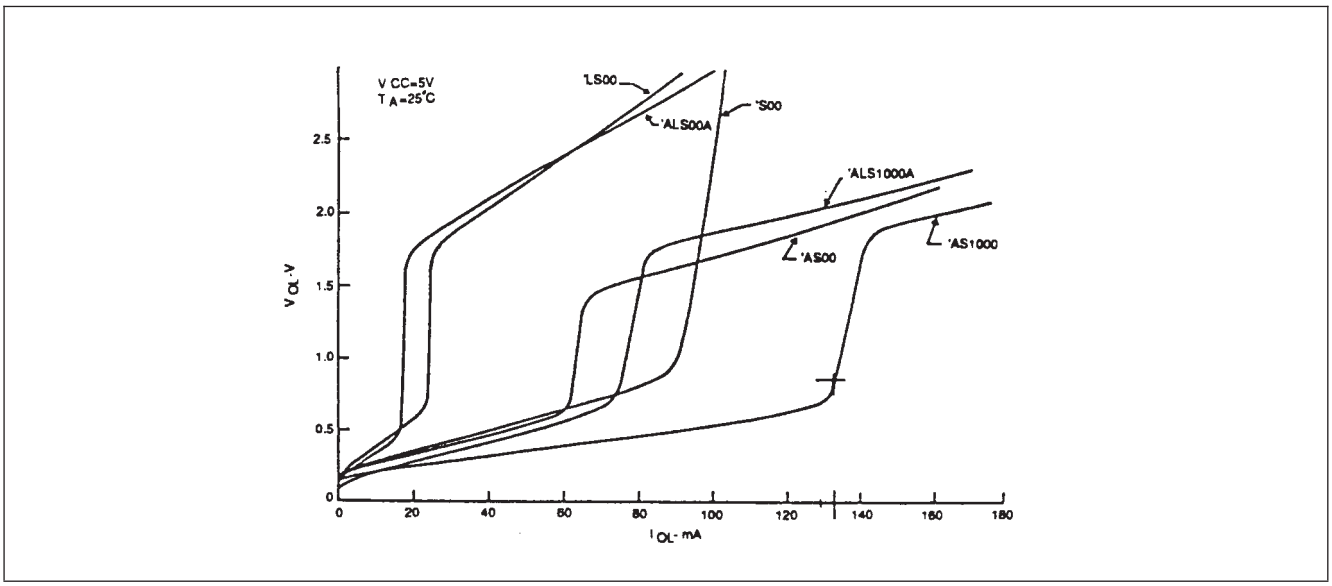


Figure A.39 74ALSxxx V_{ol} vs. I_{ol}

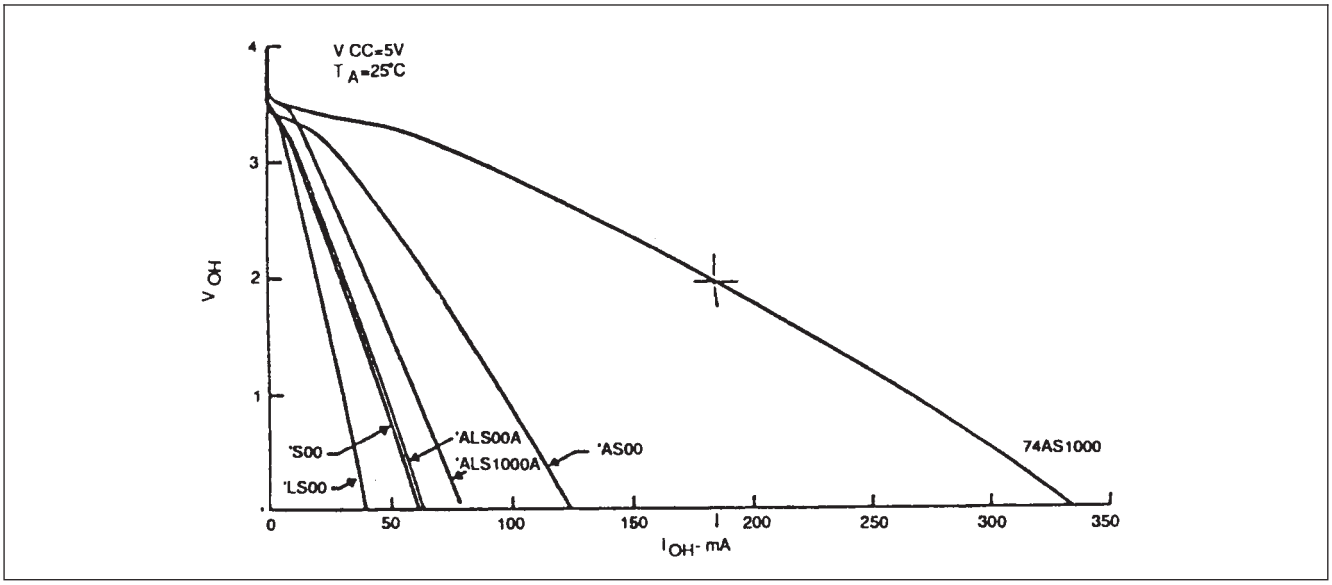


Figure A.40 74ALSxxx V_{oh} vs. I_{oh}

A.5.2 74ALSxxx AC Characteristics

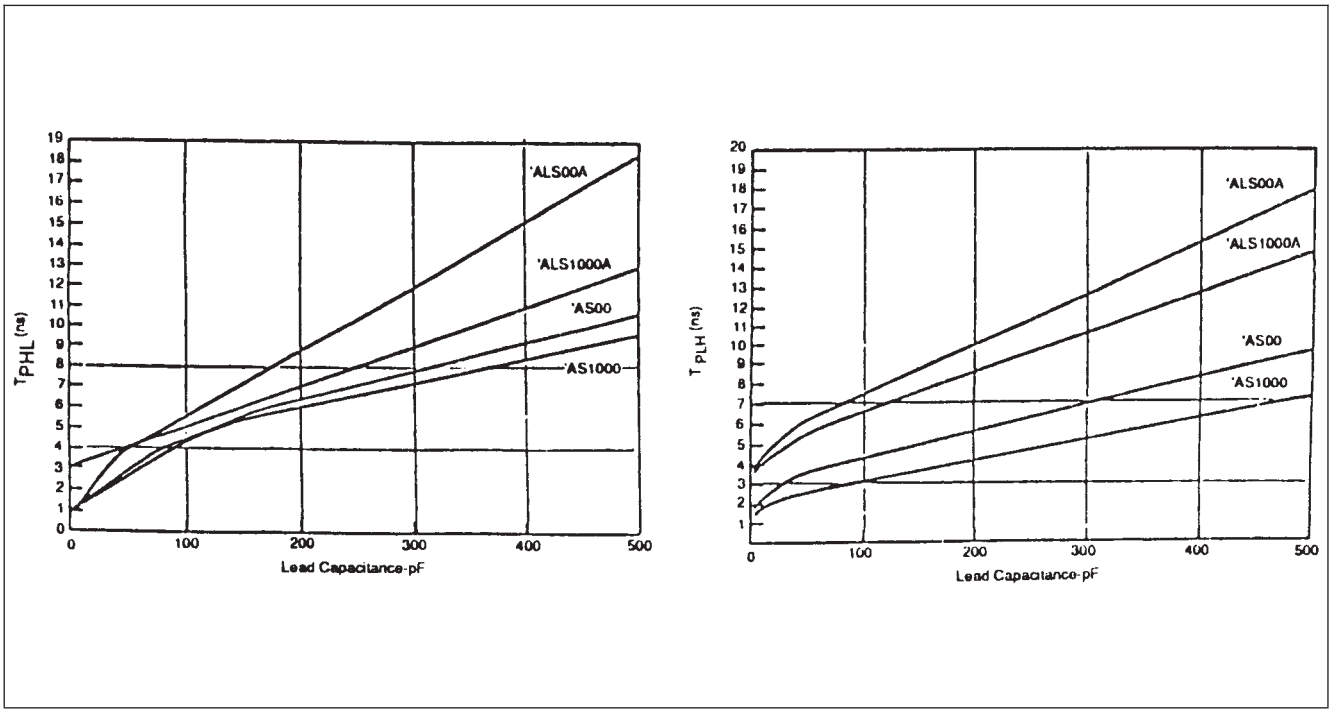


Figure A.41 74ALSxxx Propagation Delay Vs. Load Capacitance

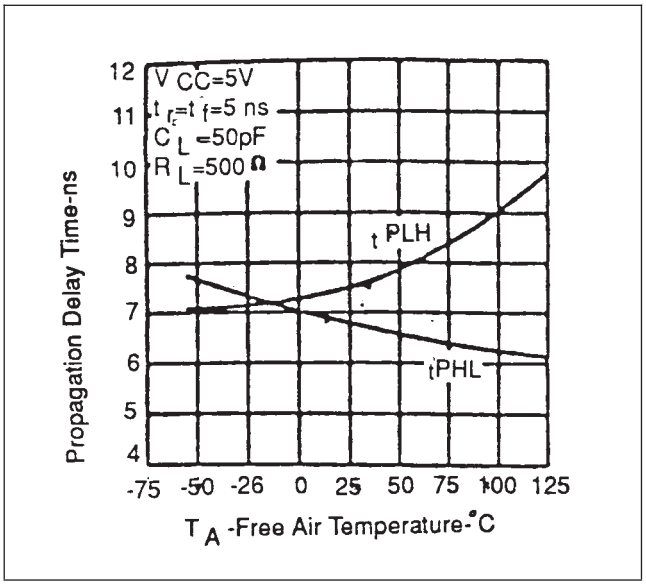


Figure A.42 74ALSxxx Propagation Delay vs. Temperature

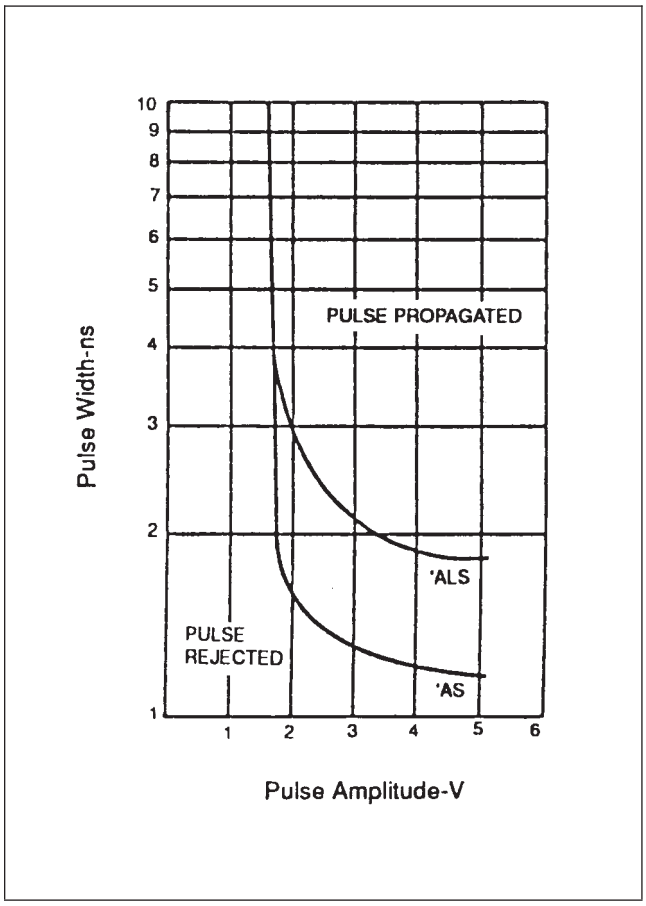


Figure A.43 74ALSxxx Noise Immunity

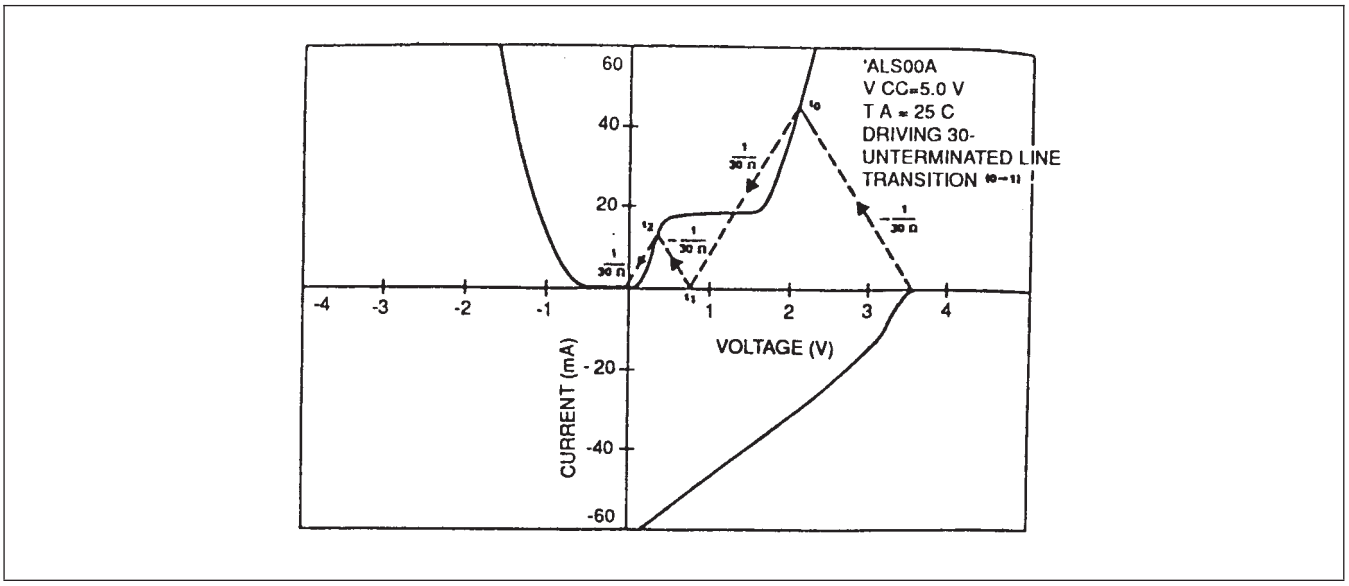


Figure A.44 74ALSxxx Bergeron Plot

A.5.3 74ALSxxx Power Dissipation

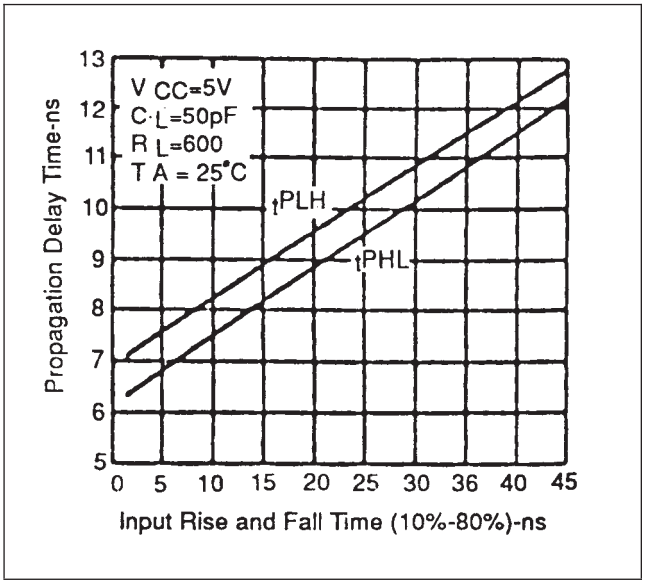


Figure A.45 74ALSxxx V_{pd} vs. T_r

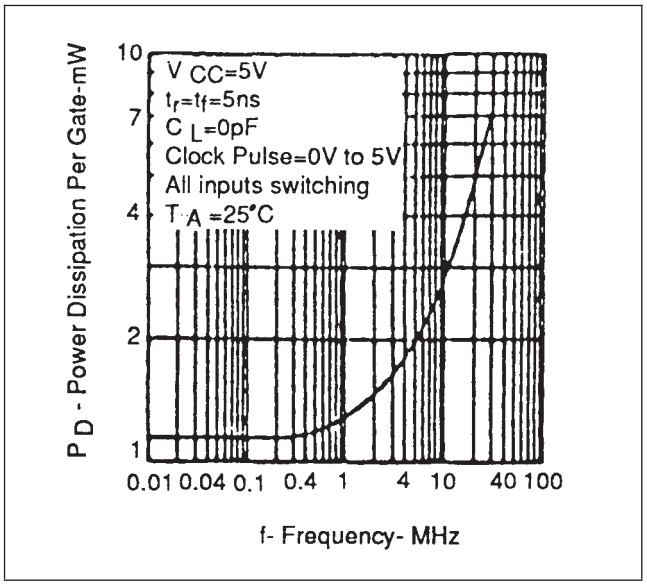


Figure A.46 74ALSxxx Power Dissipation vs. Frequency

A.6 CMOS

A.6.1 CMOS DC Characteristics

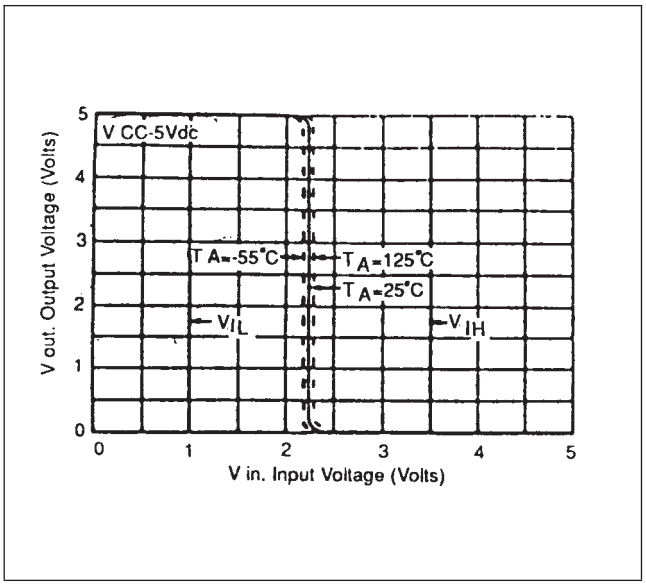


Figure A.47 CMOS V_o vs. V_i

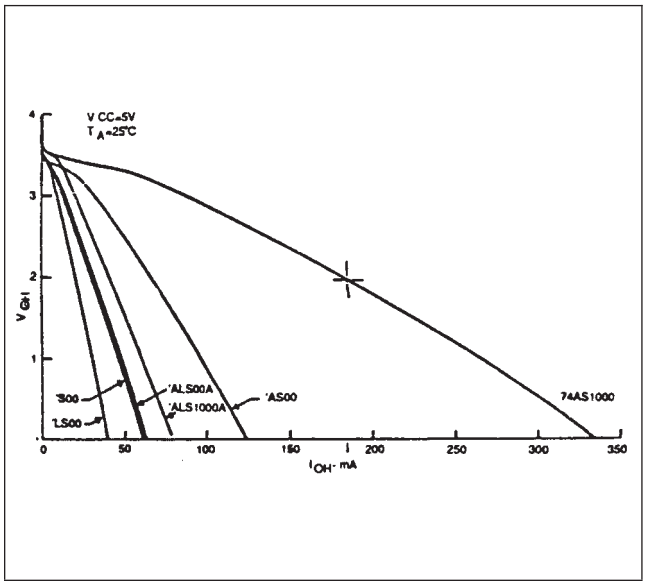


Figure A.49 CMOS V_{oh} vs. I_{oh}

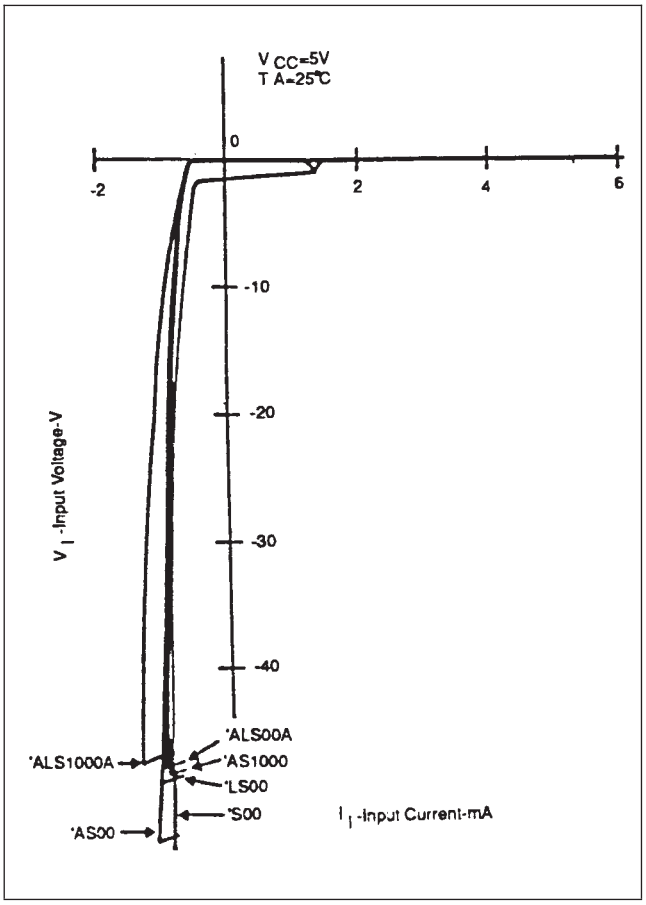
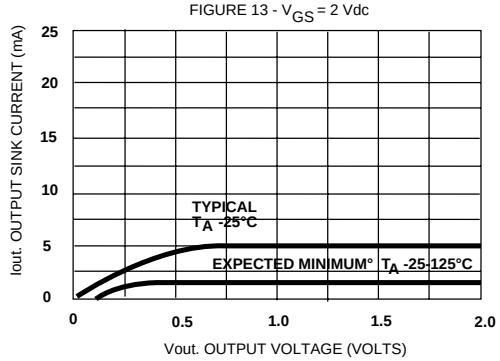


Figure A.48 CMOS V_i vs. I_i

STANDARD OUTPUT CHARACTERISTICS

N-CHANNEL SINK CURRENT

FIGURE 13 - V_{GS} = 2 Vdc



P-CHANNEL SOURCE CURRENT

FIGURE 14 - V_{GS} = -2 Vdc

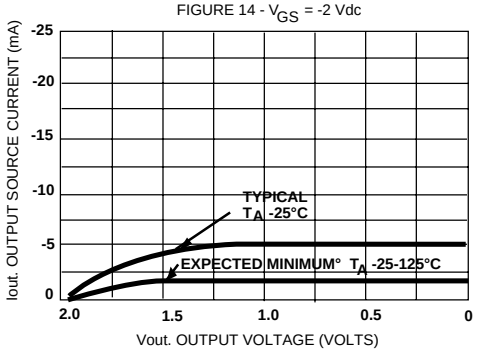
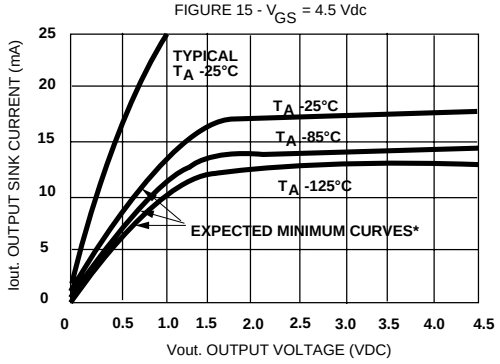


FIGURE 15 - V_{GS} = 4.5 Vdc



A

FIGURE 16 - V_{GS} = -4.5 Vdc

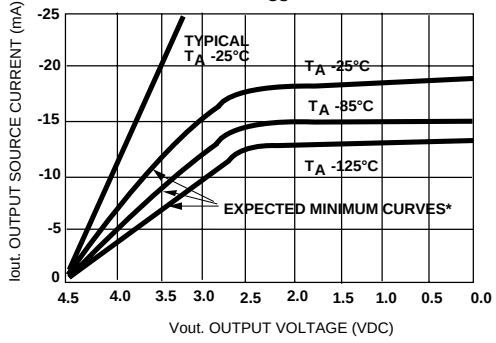


FIGURE 17 - V_{GS} = 6.0 Vdc

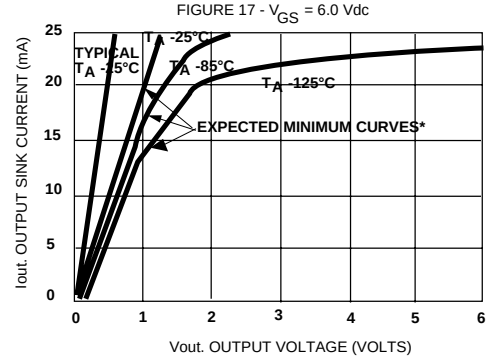
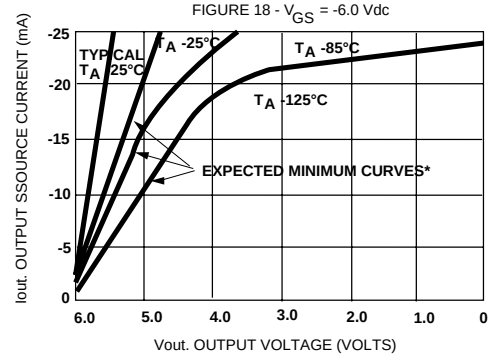


FIGURE 18 - V_{GS} = -6.0 Vdc



*** THE EXPECTED MINIMUM CURVES ARE NOT GUARANTEES, BUT ARE DESIGN AIDS.**

Figure A.50 CMOS V_{ol} vs. I_{ol}

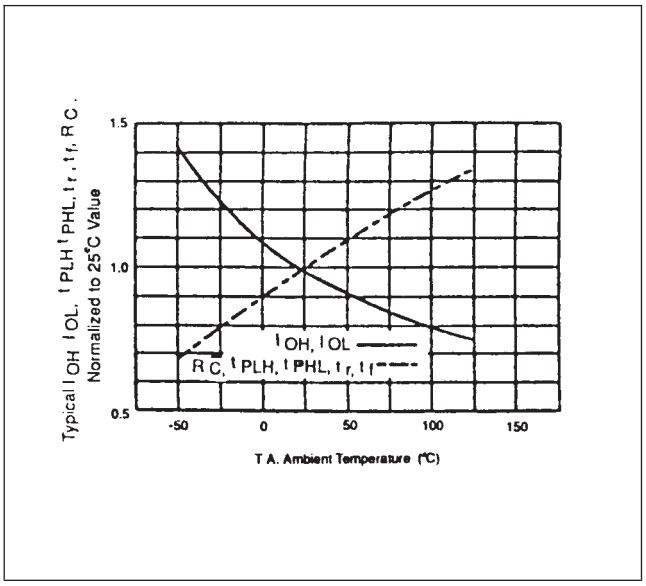


Figure A.51 CMOS I_{ol} vs. Temperature

A.6.2 CMOS AC Characteristics

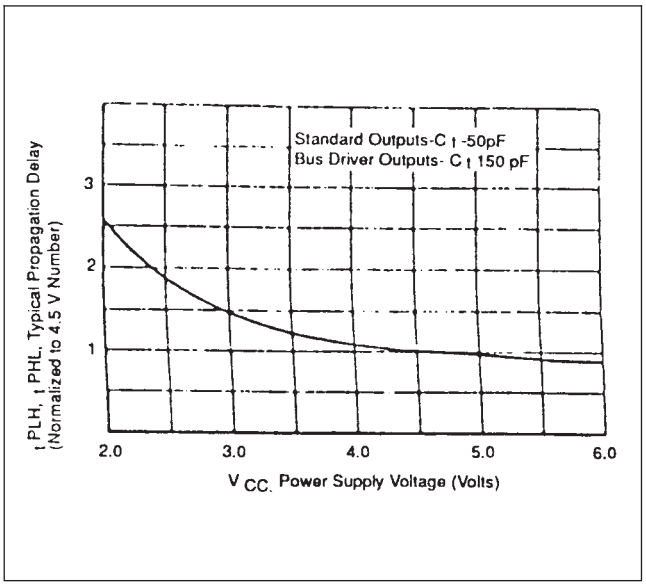


Figure A.52 CMOS Propagation Delay vs. Vcc

A.6.3 CMOS Power Dissipation

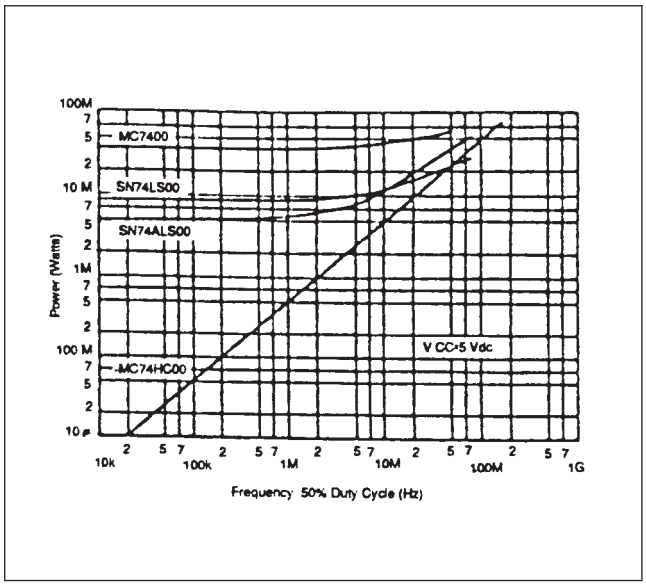


Figure A.53 CMOS Power Dissipation vs. Frequency

A.7 10K ECL Emitter Coupled Logic (ECL) keeps the signal in the linear operating region. The signal transition rates are similar to 74Sxxx, but the pulse height is only 600 mV. This logic has fast propagation times and consume more power than 74Sxxx. 10K ECL is typically slower than 100K ECL. These are bipolar devices packaged in DIP and SM Packages.

A.7.1 10Kxxx DC Characteristics

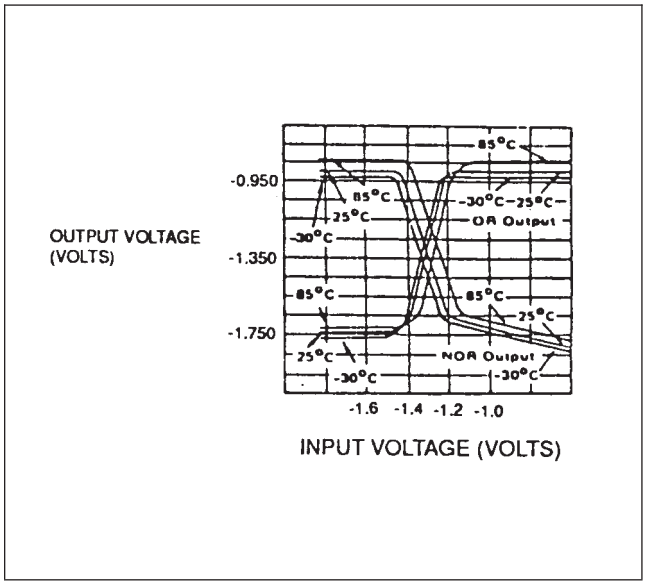


Figure A.54 10Kxxx V_o vs. V_i

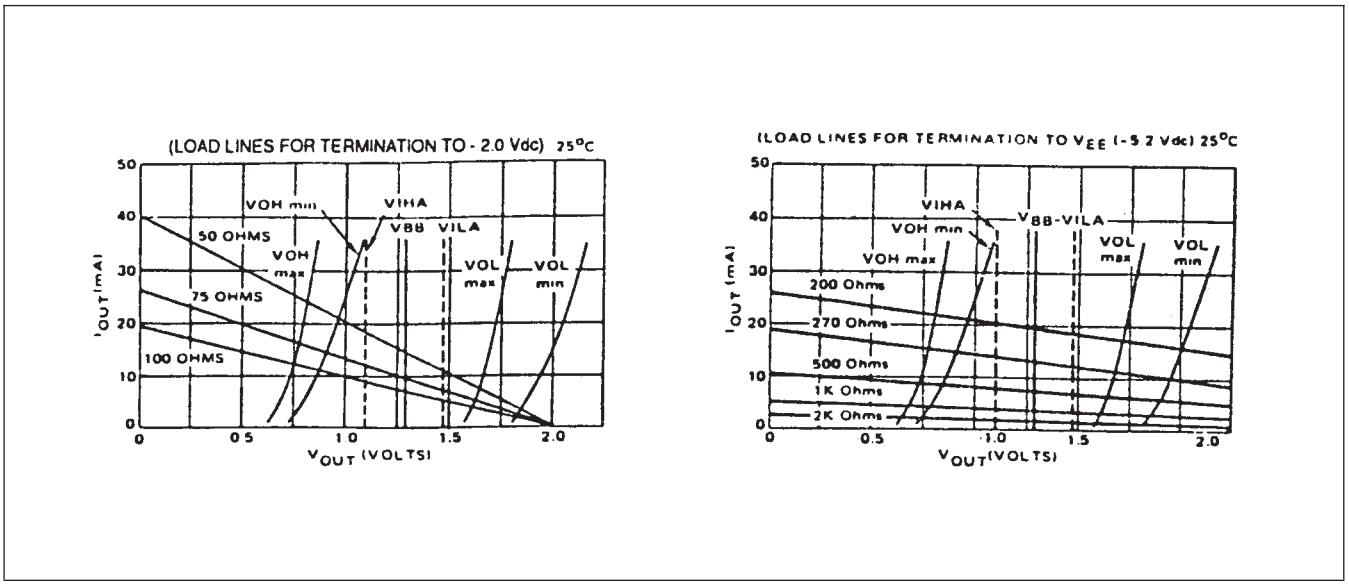


Figure A.55 10Kxxx V_{ol} vs. I_{ol}

A.7.2 10Kxxx AC Characteristics

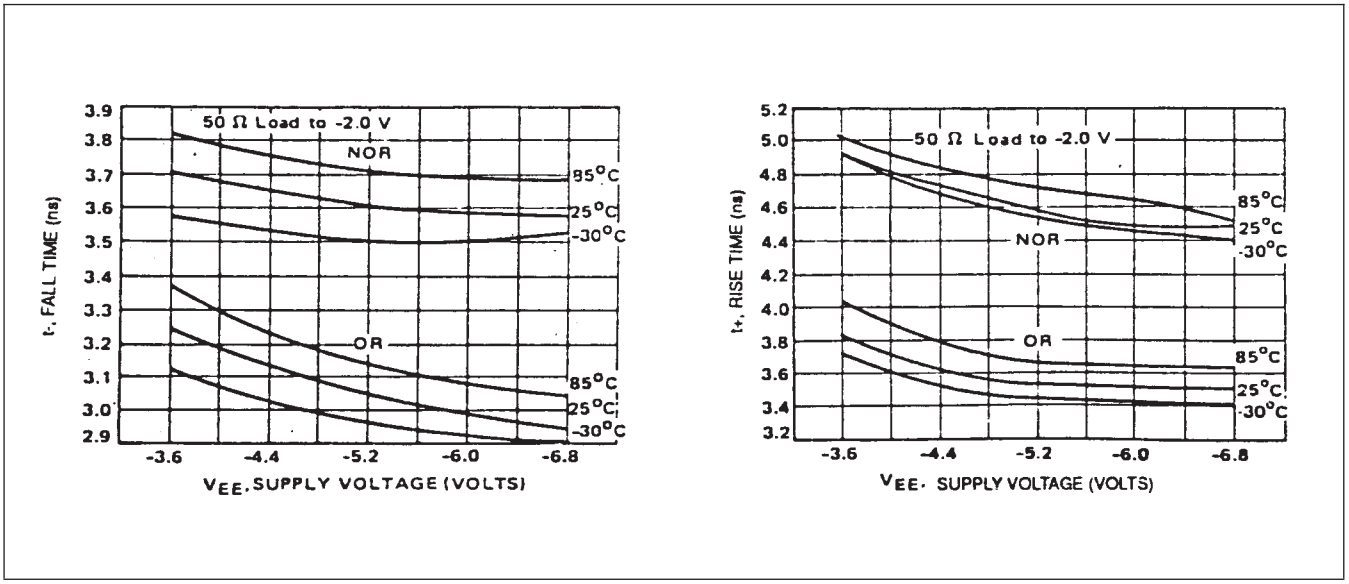


Figure A.56 10Kxxx Propagation Delay vs. Input Risetime

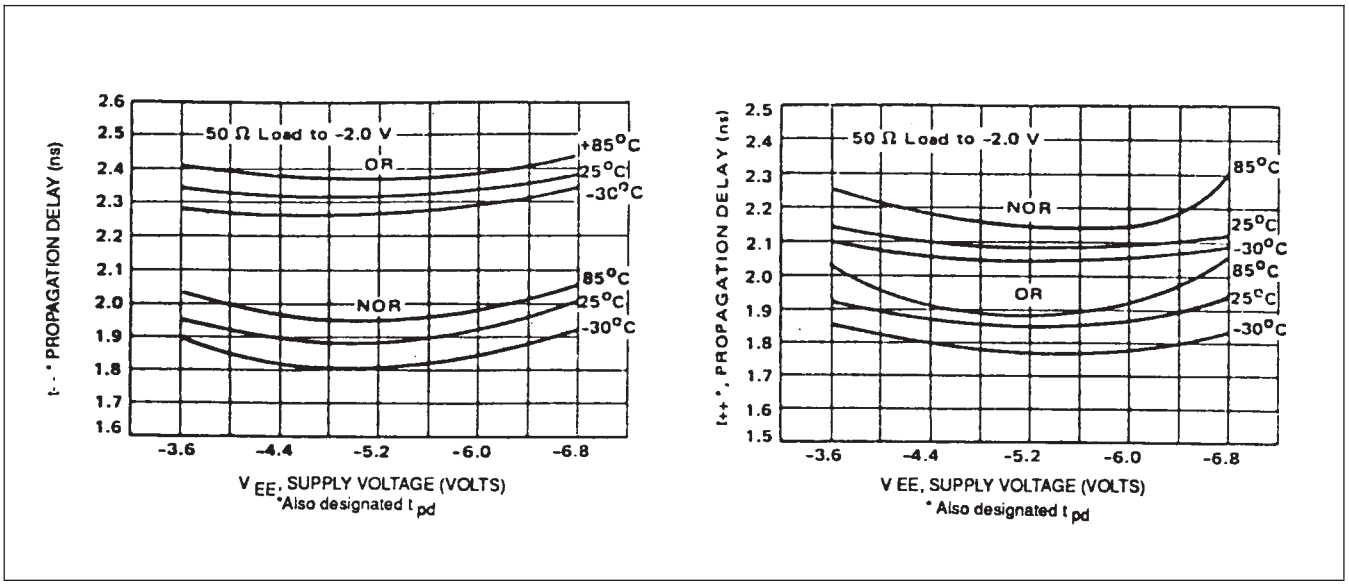


Figure A.57 10Kxxx Propagation Delay vs. Temperature

A.7.3 10Kxxx Power Dissipation

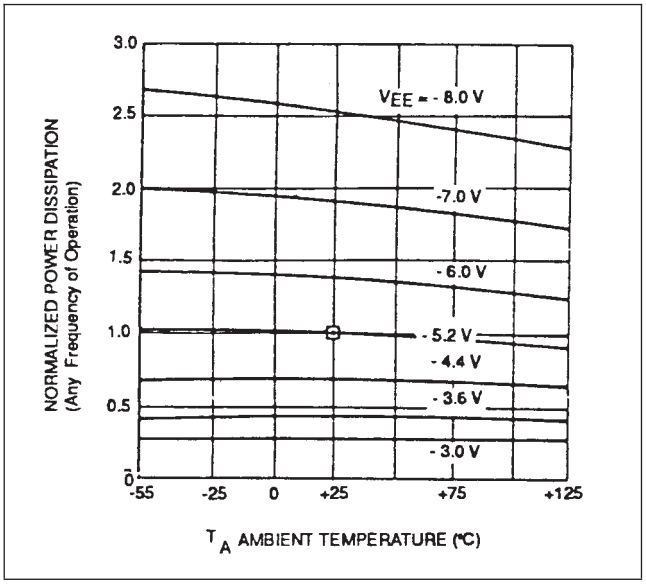


Figure A.58 10Kxxx Power Dissipation vs. Temperature and V_{EE}

A.8 100Kxxx Emitter Coupled Logic (ECL) keeps the signal in the linear operating region. The signal transition rates are faster than 10K, but the pulse height is only 400mV. This logic has fast propagation times and consumes more power than 10KECL. 100K ECL is typically faster than 10K ECL. These are bipolar devices packaged in DIP and SM packages.

A.2.1 100Kxxx DC Characteristics

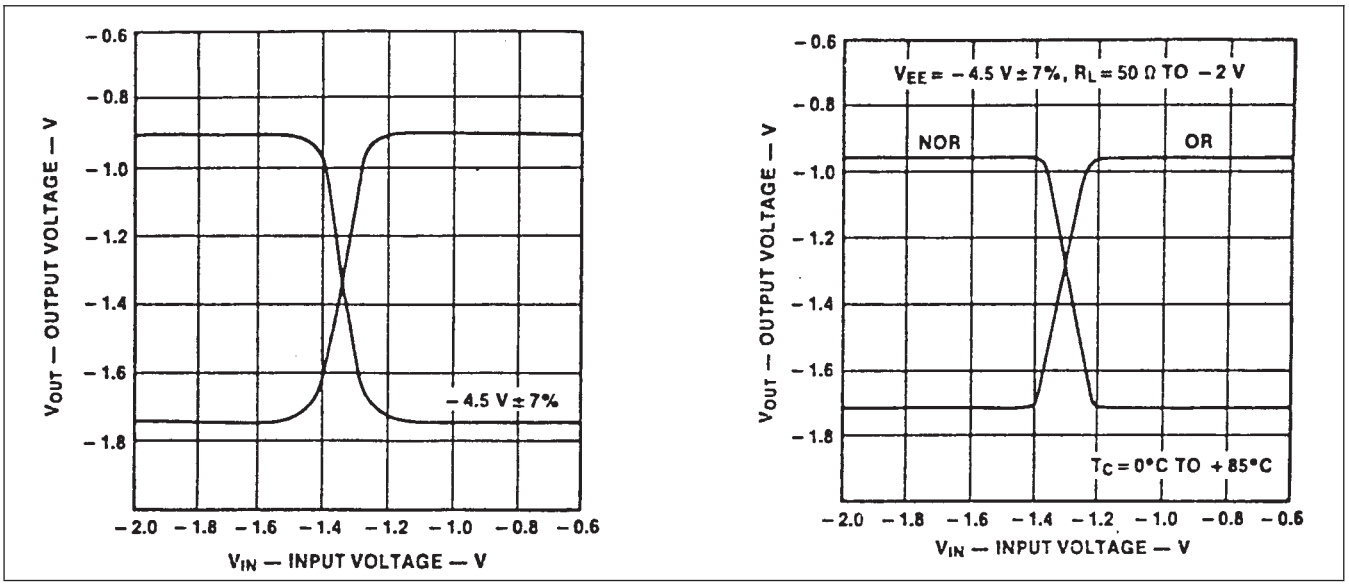


Figure A.59 100Kxxx V_o vs. V_i

Appendix B

Material Properties

Material Designation	ε_r (C-24/23/50)	Tan δ (C-24/23/50)	H_2O ABS. (D-24/ 23 Mg)	Thermal Transition		
				Tg (C)	Melting Point (C)	Other (C)
Glass-filled polysulfone resin (10% fill) (@ 10 GHz)	3.3	0.008	25	—	105	—
Mineral filled polysulfone resin (10% filling) (@ 10 GHz)	3.2	0.008	18	—	105	—
Nonreinforced polyetherimide resin (@ 10 Ghz)	3	0.006	18	—	215	—
Glass reinforced polyetherimide resin (10% filling) (@ 10 GHz)	3.4	0.008	19	—	215	—
Woven glass/epoxy resin (@ 1 MHz)	4.7	0.035	18	130	—	—
Woven glass/polyimide resin (@ 1 MHz)	4.4	0.025	35	260	—	—
Woven glass/cyanate resin (@ 1 MHz)	3.7	0.01	20	245	—	—
Woven glass/bismaleimide-triazine resin (@ 1 MHz)	4.1	0.02	18	180	—	—
Woven expanded PTFE/epoxy resin (@ 10 GHz)	2.8	0.016	18	130	—	—
Woven expanded PTFE/polyimide resin (@ 1 MHz)	2.8	0.015	35	260	—	—
Woven expanded PTFR/bismaleimide-triazine resin (@ 1 MHz)	2.8	0.016	18	180	—	—
Woven expanded PTFE/cyanate ester resin (@ 10 GHz)	2.4	0.01	15	245	—	—
Nonwoven glass/PTFE resin (@ 1 MHz)	2.25	0.001	6	—	327	19
Nonwoven glass/PTFE resin (@ 10 GHz)	2.25	0.0015	5	—	327	19
Woven glass/PTFE resin (@ 1 MHz)	2.55	0.005	8	—	327	19
Woven glass/PTFE resin (@ 10 GHz)	2.5	0.003	8	—	327	19
Woven glass/PTFE (high content) (@ 10 GHz)	2.25	0.002	8	—	327	19
Nonreinforced PTFE resin (.010 thick) (@ 10 GHz)	2.1	0.001	1	—	327	19
Filled PTFE resin (mid range) (@ 10 GHz)	6	0.003	13	—	327	19
Filled PTFE resin (high range) (@ 10 GHz)	10	0.003	7	—	327	19
Nonreinforced polyethersulfone resin (@ 1 GHz)	3.4	0.01	28	—	230	—
Nonreinforced polysulfone resin (@ 10 GHz)	3	0.008	20	—	105	—

Appendix C

TUTORIAL

C.0 System Electrical Design Concepts

C.1 Electromagnetic Wave Signals Propagation Versus Electric Current in Conductors Interconnection and the packaging of electronic components primarily have been the domain of mechanical designers who were concerned with such factors as weight, volume, power, cooling, form factor and environmental constraints, with interconnections specified in wire listing or to/from listings. Conductors of electrical signals were routed with only two concerns: that continuity was maintained between points and that no shorts were permitted. Aside from providing a good electrical path, the electrical properties of the signal were not a major concern.

However, recent advances in digital integrated circuits have introduced new devices with extremely fast rise times housed in high density microelectronic packages. In order to optimize system performance, these devices require a wiring technology that supports high density interconnection and, at the same, provides superior electrical performance. With the market's appetite for high speed processing growing at over 30% per year, high speed digital processing is no longer the domain of a few scientific super computers. Even medium size mainframes and minicomputers are touting processing rates of more than 3 million instructions per second (MIPS) and machine clock rates of 50 to 250 MHz, and the high speed technology has penetrated the commercial, telecommunications and military markets.

While many system problems are associated with high speed digital processing, none has received more attention lately than interconnection. The reason for this attention is shown in Figure C1 where it is evident that as system speeds increase, interconnection and packaging become the bottlenecks that slow system performance. Systems using 100K ECL circuitry have almost 55% of the system delay in the packaging and interconnection. This situation is even worse when GaAs technology is utilized. CMOS is normally considered a ''slow'' technology, but is now being designed into system clock rates in excess of 100 MHz. In these cases, not only is system delay a problem but signal attenuation becomes an issue with the low powered CMOS devices.

What is the fundamental phenomena that imposes the special treatment for the so called ''high speed digital'' interconnections? We have come to assume that signal routing and the routing of electrons in the form of current and voltages are synonymous. However, at the higher speeds, more and more energy is propagated as electromagnetic waves. Resistance must now be thought of as resistance to electro-magnetic wave, which is the alternative item for impedance. Instead of voltages and current, we now must think in terms of electric and magnetic fields. The parameter that affects the electric field is called capacitance and that affecting the magnetic field, inductance, but more specifically self-inductance. Self means the value is determined by the conductor itself. On the other hand, capacitance is determined by relationship between conductors and the surrounding medium. Consequently, from the design standpoint, we are designing to specific impedance values by trying to control the capacitance and inductance with line width and thickness variations, dielectric thicknesses, aspect ratios and the relative permittivity of the material between conductors as transmission lines. Signal paths must be kept short to minimize propagation delays. Even if it were possible to make a circuit capable of switching at infinite speed, it would be the interconnection that would dictate the performance of the systems using these devices. Figure C2 illustrates the switching speed of a device (i.e., transistor) vs. propagation delay in a medium commonly used in the printed board industry. This can also be plotted for hybrid ceramic circuits, silicon mother boards and other means of signal[1] transport.

The plot shows the immediate degradation of the device performance due to the limitation of signal propagation delays through a common interconnection medium. Note that the simplest possible system configuration has been assumed, i.e., one flip-flop sending a signal to another. Even under these unrealistically simplified conditions, the two flip-flop system-using devices with infinite switching speeds could not operate any faster than 1 GHz if the signal is transmitted through 6″ of printed board material, 4″ of ceramic or 3″ of silicon. If the switching devices were rated 1 GHz, travel through 6″ of printed board material will cut the speed in half to 500 MHz.

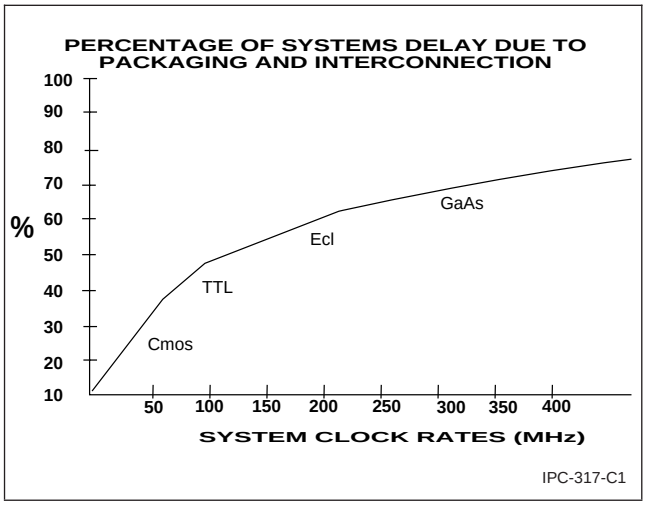


Figure C1 Propagation delay due to packaging effects

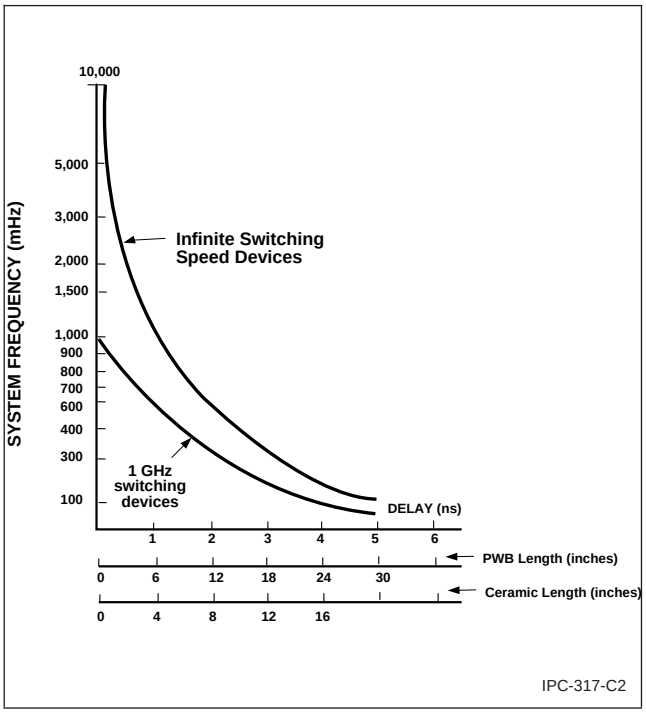


Figure C2 System speed vs. signal growth length

The conclusion of these considerations is that a close interrelationship between mechanical design and electrical performance exists in the case of interconnection lines involving high speed digital signals. This interdependence did not exist or it could be ignored in low speed signal applications and it imposes new design rules, restrictions and process controls.

To meet the challenges of high speed digital processing, today's circuit board must:

– reduce propagation delay;

– lower crosstalk and other line parasites;

– reduce signal loss; and

– allow high and very high density interconnections.

It is important to mention here that these specific requirements must be accomplished on top of all the other mechanical and electrical specifications as defined for the existing technologies already in use.

To achieve these desired goals the designer must start by controlling the impedance of the transmission lines on the board. For this reason, the circuitry used in high speed digital applications is known under the generic name of ''Controlled Impedance Packaging''.

C.2 Critical Signal Speed At what frequencies should there be concern about wave propagation rather than just current in conductors? The general rule is that transmission line effects (wave effects) become an important design consideration when the length of the interconnection approaches 1/7 of the wavelength of the signal being transported. If the system clock frequency is 300 MHz, the wavelength in air is about 1 m.

Unfortunately, this is not the frequency of concern. Generally, the system clock is a repetition rate of a square wave pulse. Most systems will be digital and the information as to whether the pulse is a ''1'' or a ''0'' is carried in the leading edge of the pulse (the sharp rise). This edge must be permitted to rise (or fall) as quickly as possible. Frequency and the rise time of the signal are related by the relation Tr = 0.35/f where Tr is the rise time in nsec and f is the frequency in GHz.

A method of determining the required rise is to examine the type of devices that need to be interconnected. Table C1 shows the rise times values for some of the most popular high speed IC's.

Table C1 Rise Time

Device Family	Output Pulse Rise Times (nsec)
TTL	6–9
Schottky TTL	2–3
ECL	0.45–0.75
GaAs	0.05–0.20

For example, ECL has a 0.45 rise time with a corresponding frequency of concern of 0.35/0.45 GHz or 777 MHz. This translates to a wavelength in air of about 15″, 7.5″ in FR-4 or less than 4″ in ceramic. This means that for circuit boards fabricated from FR-4, if the interconnection path is more than 1.0″, the electromagnetic properties of the signal, and the waveguide or transmission line effects should be considered.

From this example, it becomes obvious that the critical signal speed is the signal rise/fall time instead of the clock frequency.

C.3 Transmission Line Effects

C.3.1 Signal Propagation Delay It is easy to understand this phenomena if we consider the propagation of an electromagnetic wave through a insulator medium as the model of signal transmission in a ''high speed'' board. The propagation speed of an electromagnetic wave is related to the permittivity of the insulating medium by the relation $v_P = c/(\varepsilon_r)$, where c is the velocity of light (3×10^8 m/sec) and ε_r is the permittivity of the insulating material. The permittivity of polyimide is about 3.5, glass epoxy for printed board is 4 to 5, hybrid ceramic is 9-10 and that of silicon wafers is about 15. To preserve the speed of high speed devices, we must think in terms of total interconnection lengths.

Generally speaking, one can say that for ECL circuits with terminated lines, the propagation velocity varies inversely with the square root of the line capacitance and for CMOS circuits, where the delay is caused by skew, the speed varies inversely with the capacitance.

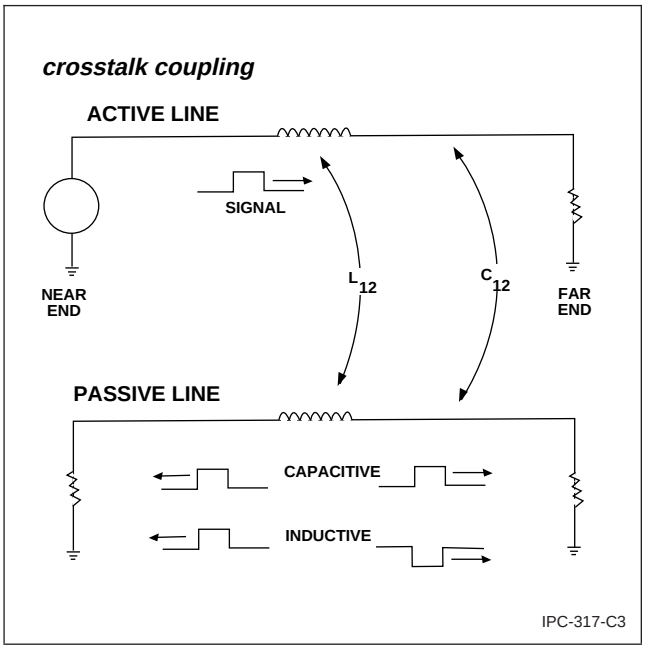


Figure C3 Crosstalk coupling

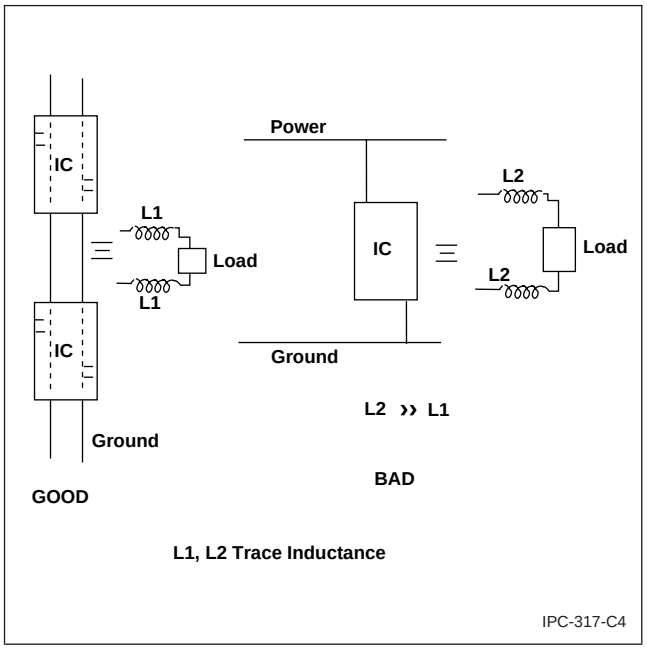


Figure C4 Power/Ground interconnections

C.3.2 Crosstalk Crosstalk is the transfer of energy between adjacent circuits via capacitive or inductive coupling. The energy from the ''source'' circuit becomes superimposed on the ''receptor'' circuit signal leading potentially to malfunction of the logic, including spurious switching and circuit drop-outs. Figure C3 represents two adjacent uniform signal lines, one of which carries a pulse-type signal. The coupling between the two lines is by mutual inductance and capacitive components L_{12} and C_{12}, respectively. Signals introduced into the active line will be induced into the quiet or passive line by electromagnetic fields that accompany the traveling signal on the active line. The near end refers to the signal originating end, the far end, the signal receiving end. It is assumed that the active and quiet line both have good returns to ground.

If the magnetic coupling is separated from the capacitive coupling between the active and passive lines, different phenomena occur. The coupled signals going toward the far end are called forward crosstalk and the coupled signals in the passive line coming back to the near end are called backward crosstalk. The coupling due to capacitive effects (that due to the electric field) causes a smaller replica of the active signal to be sent to both the far and the near ends, with the same polarity as the active signal.

The coupling due to the inductive effects (that due to the magnetic field) also sends signals to both the near and the far ends, but the signal to the far end is inverted (opposite polarity) to that of the active signal. Consequently, the backward crosstalk composite of the inductive and capacitive coupling is the sum of signals, but the forward crosstalk composite is the difference between the two signals, usually resulting in a smaller component. Therefore, the crosstalk coupling coefficient found in references is different for the two.

The degree of isolation required of crosstalk for systems is usually specified as 60 dB for analogue type signals and 26 dB for digital signals.

The most common techniques of reducing crosstalk effects in high density circuits are as follows:

a) to increase the separation;

b) to reduce the parallel length;

c) to reduce the line impedance;

d) to reduce the signal level;

e) to interspace signal traces with ground trace

C.3.3. Switching Noise When gates are switching, current is either drawn or passed to the power supply through the power/ground links. When this current has high frequency components, the self-inductance of the leads and traces become significant, leading to transient or switching noise. These transients are related to the inductance of power/ground loop and hence this layout must be designed so as to reduce this inductance as much as possible. Hence, the layouts shown in Figure C4 give good and bad layouts for the power/ground interconnection.

A common technique to reduce switching noise is the use of decoupling capacitors that serve to provide the current from a point closer to IC than the power supply. Even when this is done, the positioning of the capacitor is important, as shown in Figure C5. If the capacitor leads are too long, the self inductance becomes too high leading to the common switching noise.

The decoupling on DIP boards is normally achieved with discrete capacitors that can be closely positioned to the IC. For

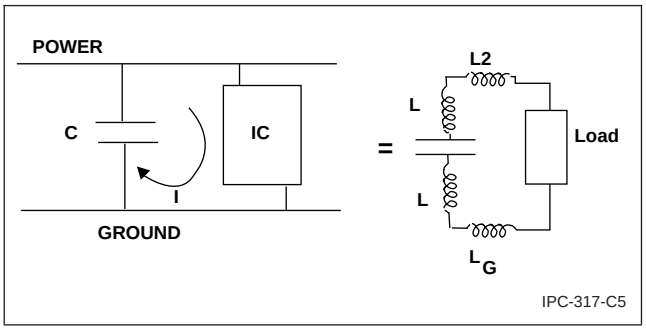


Figure C5 Decoupling capacitor placement

the higher I/O packages, a trend has started that is to place the decoupling capacitor in the package as shown in Figure C6. This has the double advantage of not using real estate for the capacitor and reducing the size of the capacitor interconnections. Closely spaced adjacent power/ground planes are also being utilized to provide high frequency decoupling capacitance. This also decreases the real estate required for decoupling capacitors.

C.3.4. Other Parasitics Noise Multilayer circuit boards have obvious advantages over double sided boards in the sense that the power/ground are continuous layers of metallization. Consequently, they offer a lower r.f. impedance to the spurious currents and the current distribution is such that the current in the return circuit follows the conductor wire path as shown in Figure C7.

This means that the current loop is significantly reduced in area since the area is now bounded by the signal wire length and the separation between signal layer and the ground or decoupled power layers. To further enhance the multilayer improvement, adjacent layers (signal) can be run orthogonally thus reducing the crosstalk. The power and ground layers will also serve to shield emissions.

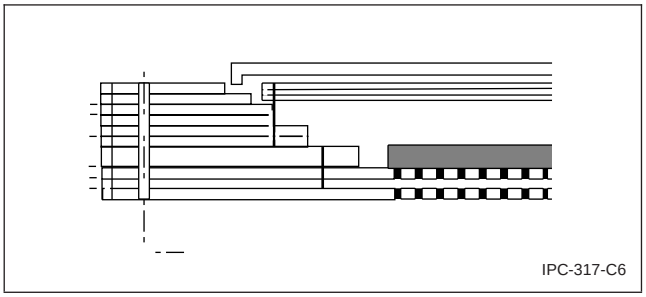


Figure C6 High I/O component decoupling capacitor design

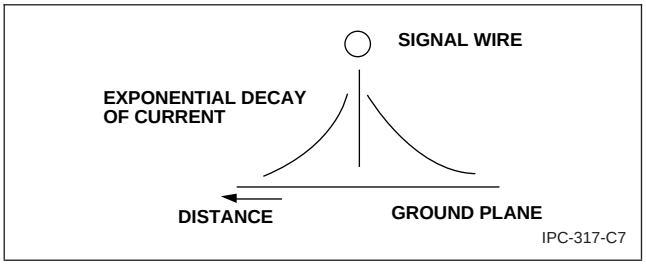


Figure C7 Current distribution in ground plane

C.3.5 Noise Budget/Noise Margin

In Section 5.0, we described the transmission line effects that interfere with the original electrical signal and modify it as it passes through the interconnection. This modification of the original signal may effect the performance of the system. But what are the limits in which the characteristics of the original signal can be modified and the system will continue to perform properly? This concept is called the ''Noise Budget''.

A noise budget is defined as the allocation of a voltage tolerance for the system DC and AC voltage drops for a device to operate within specific boundaries. There are two primary system noise budgets. The first is the DC power supply noise budget for each IC. The second is the device logic signal AC noise budget.

Each logic device connects to a positive voltage and a ground return. The system power distribution has finite AC and DC voltage drops between the power supply and component. Also, the power supply has a designated operating tolerance. The logic device must operate over an input voltage range of V_{CC} ±NM, where NM is the noise margin. The primary components that are allocated for the noise margin are:

a) Power supply tolerance

b) System DC drops

c) Bulk decoupling drops

d) IC decoupling drop

e) Component input voltage tolerance

f) Preset power supply voltage

These concepts are presented in detail in Chapter 5.

C.4 High Speed Electronics Packaging Design—Concept and Methodology We can conclude at this point with the fact that, if the requested digital signal speed is higher than the critical speed (as defined in section 3.2), the transmission line effects interfere with the original signal creating delay and distortions. On the other hand, the capability of electronic devices to function properly when distorted signals and noises are propagated through the system is limited by their noise margin characteristics. A good packaging engineer must create a physical design in which the errors introduced by the transmission line effects are compatible with the noise budget of the system being created.

Although the concept sounds simple enough, one should not forget that a designer has to accommodate this requirement in a world in which another large number of restraints is already imposed from the type of system to design, from the technology to be implemented or simple limitations imposed by the material properties available in the market. These limitations leave to the packaging designer a narrow path in which he can find few options.

Appendix D

CIRCUIT BOARD LAYUPS

D.1 Common Printed Circuit Board Layups The following figures present typical multilayer printed circuit board layer constructions. These provide microstrip, stripline and dual stripline transmission line configurations. For optimum EMI performance, the highest frequency signals should be placed on internal layers below reference planes. Power distribution planes should be close to each other to provide maximum distributed capacitance for decoupling high speed signals.

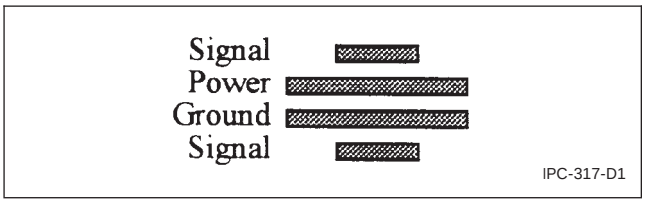


Figure D1 4 Layer

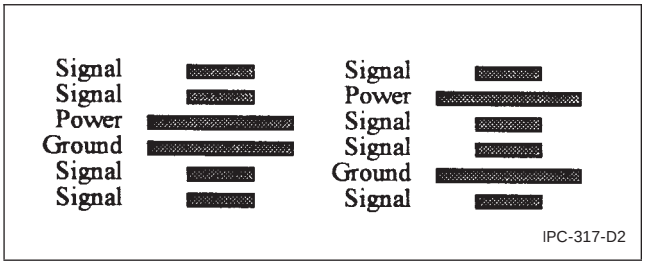


Figure D2 6 Layer

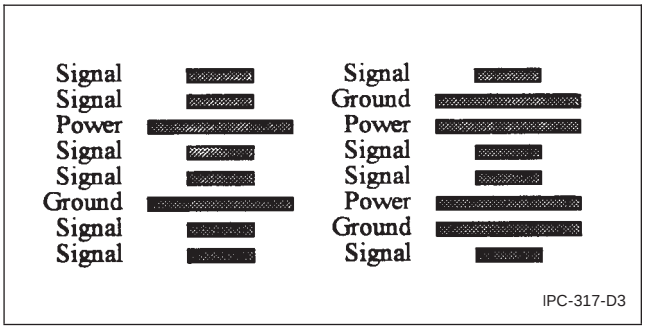


Figure D3 8 Layer

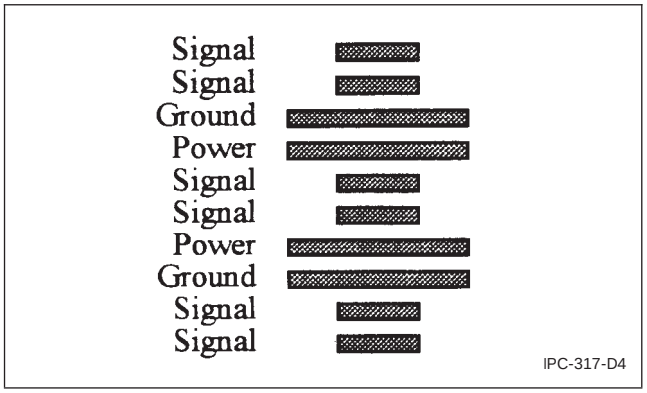


Figure D4 10 Layer

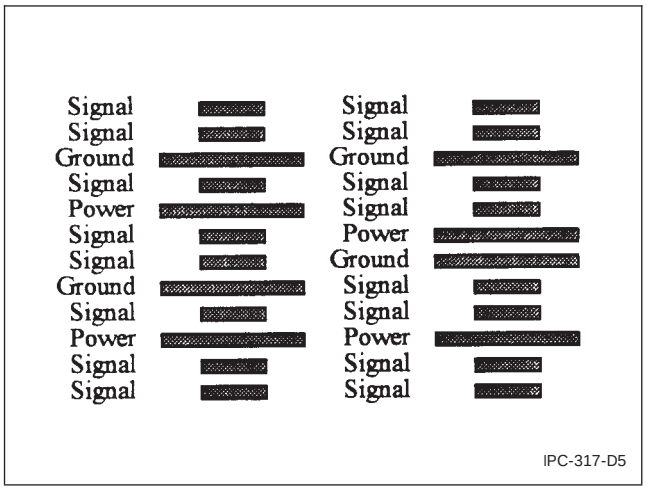


Figure D5 12 Layer

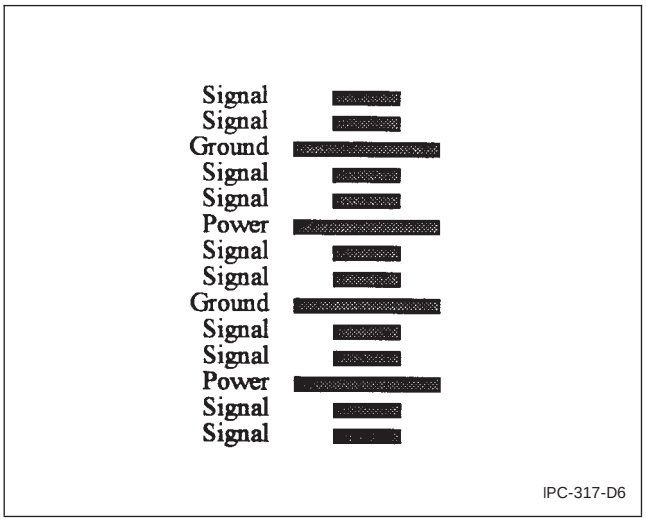


Figure D6 14 Layer

D.2 Common Discrete Circuit Board Layups The following figures present typical discrete wiring circuit board layer constructions. These provide microstrip, stripline and dual stripline transmission line configurations. For optimum EMI performance, the highest frequency signals should be placed on internal layers below reference planes.

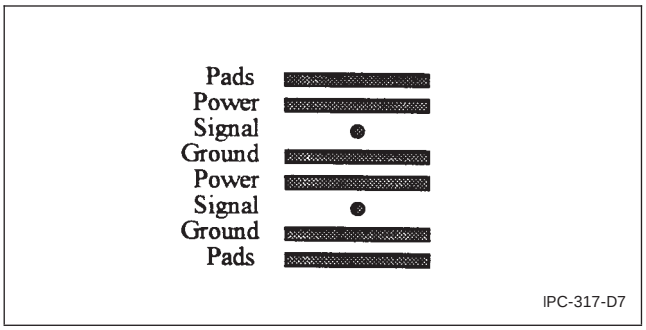


Figure D7 8 Layer

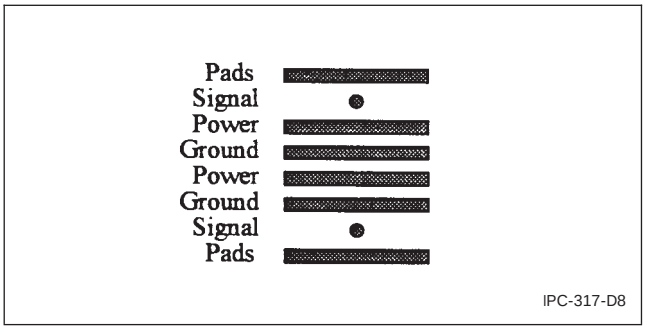


Figure D8 8 Layer; ML Core

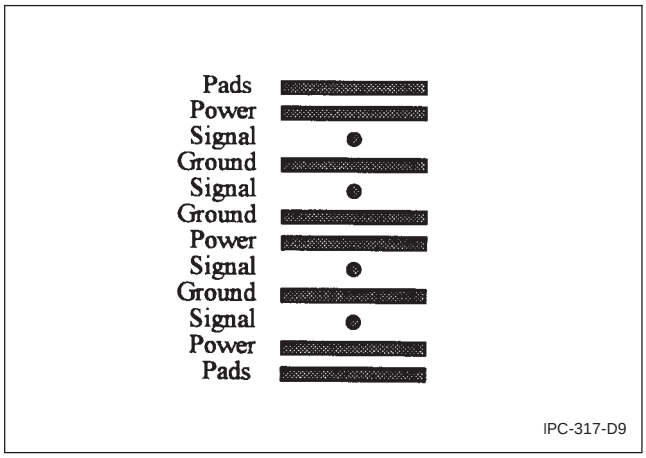


Figure D9 12 Layer

Appendix E

BIBLIOGRAPHY

Impedance Calculation

G.L. Matthaei, et al., ''Microwave Filters, Impedance-Matching Networks, and Coupling Structures'', McGraw-Hill Book Co., New York, 1964, p. 168-196.

H. Howe, Jr., ''Stripline Circuit Design'', Artech House, Dedham, MA 1974.

J.P. Shelton, ''Impedances of Offset Parallel Coupled Strip Transmission Lines'', IEEE Trans., Vol. MTT-14, Jan. 1966, p. 7-15; Correction, MTT-14, May 1966, p. 249.

R.R. Gupta, ''Fringing Capacitance Curves for Coplanar Rectangular Coupled Bars:, IEEE Trans., Vol. MTT-17, 1969, p. 637-638.

H.J. Riblet, ''Two Limiting Values of the Capacitance of Symmetrical Rectangular Coaxial Strip Transmission Line'', IEEE Trans., Vol. MTT-29, July 1981, p. 661-666.

S. Rimmon, ''Master the Challenge of Offset Stripline Design'', Microwaves, Vol. 15, May 1976, p. 40-44.

D.K. Larson, ''Computer Plotter = Direct-to-Art Design'', Microwave, Vol. 20, March 1981, p. 91-97.

H.E. Green and J.R. Pyle, Jr., ''The Characteristic Impedance and Velocity Ratio of Dielectric Supported Strip Line'', IEEE Trans., Vol. MTT-13, Jan. 1965, p. 135-136.

H. Howe, Jr., ''Dielectrically Loaded Stripline at 18 GHz'', Microwave Journal, Volume 9, Jan. 1966, p. 52-54.

J.K. Richardson, ''An Approximate Formula for Calculating the Characteristic Impedance of a Symmetric Stripline'', IEEE Trans., Vol. MTT-15, Feb. 1967, p. 130-131.

P. Schiffres, ''How Much CW Power Can Striplines Handle?'', Microwaves, June 1966, p. 25-34.

G.D. Vendelin, ''Limitations on Stripline Q'', Microwave Journal, Vol. 13. May 1970, p. 63-69.

Ashok K. Gorwara, ''Transmission Media-What's Suitable at MM Wavelengths?'' Microwaves, Vol. 15, March 1976, p. 36-42.

E. Yamashita and S. Yamayaki, ''Parallel-Strip Line Embedded In or Printed On a Dielectric Sheet'', IEEE Trans., Vol. MTT-16, Nov. 1968, p. 972-973.

E. Yamashita and K. Atsuki, ''Stripline with Rectangular Outer Conductor and Three Dielectric Layers'', IEEE Trans., Vol. MTT- 18, May 1970, p. 238-243.

J.M.C. Dukes, ''An Investigation into Some Fundamental Properties of Strip Transmission Lines with the Aid of an Electrolytic Tank'', Proc. IEE, Vol. 103, Part B, May 1956, p. 319-333.

J.M.C Dukes, ''The Application of Printed Circuit Techniques to the Design of Microwave Components'', Proc. IEE, Vol. 104, part B, 1957, p. 155-157.

A.F. Harvey, ''Parallel-Plate Transmission Systems for Microwave Frequencies'', Proc, IEEE, Vol. 106, part B, March 1959, p. 129-140.

H. Guckel, ''Characteristic Impedance of Generalized- Rectangular Transmission Lines'', IEEE Trans., Vol. MTT-13, May 1965, p. 270-274; Correction, MTT-16, Aug. 1968, p. 555.

E. Castamagna, ''Fast Parameter Calculation of the Dielectric Supported Air-Strip Transmission Line'', IEEE Trans., Vol. MTT- 21, March 1973, p. 155-156; Correction MTT-22, April 1974, p. 474.

C.M. Weil, ''The Characteristic Impedance of Rectangular Transmission Lines with Thin Center Conductor and Air Dielectric'', IEEE Trans., Vol. MTT-26, April 1978, p. 238-242.

H.R. Kaupp, ''Characteristics of Microstrip Transmission Lines'', IEEE Trans., Vol. EC-16, No. 2 April 1967.

Coupled Transmission Lines

H. Amemiya, ''Time Domain Analysis of Multiple Parallel Transmission Lines'', RCA Review, Vol. 28, No. 6, pp. 241-276, June 1967.

I. Catt, ''Crosstalk (Noise) in Digital Systems'', IEEE Transactions on Digital Computers, Vol. EC-16, No.6, pp. 743-763, December 1967.

S.B. Cohn, ''Characteristic Impedances of Broadside Coupled Strip Transmission Line'', IRE Trans., Vol. MTT-3, Oct. 1955, p. 29-38.

C.W. Davidson, ''Transmission Lines for Communication'', John Wiley and Sons, New York, NY, 1978.

J.A. DeFalco, ''Reflections and Crosstalk in Logic Circuit Interconnections'', IEEE Spectrum, Vol. 7, No. 7, pp. 44-50, July 1970.

R. Facia and A. Wexler, ''Greenfield: General Purpose Transmission Line Simulator'', Product Data Sheets, Quantec Laboratories, Inc., Suite 200, 281 McDermot Ave., Winnipeg Canada R3B OS9, 1988. (204) 943-2552.

B.L. Hart, ''Digital Signal Transmission'', Van Nostrand Reinhold (UK), Wokingham, Berkshire, England, 1988.

O.A. Horna, ''Pulse Reflections in Transmission Lines'', IEEE Transactions on Electronic Computers, Vol. EC-20, No. 12, pp. 1558-1563, December, 1971.

D.W. Kammler, ''Calculation of Characteristic Admittances and Coupling Coefficients for Strip Transmission Lines'', IEEE Trans., Vol. MTT-16, Nov. 1968, p. 925-937.

G. Metzger and J. Vabre, ''Transmission Lines with Pulse Excitation'', Academic Press, New York, NY, 1969

V.K. Tripathi, ''Loss Calculations for Coupled Transmission Line Structures'', IEEE Trans., Vol. MTT-20, Feb. 1972, p. 178-180.

R. Pregla, ''Distributed Capacitances for Coupled Rectangular Bars of Finite Width'', AEU, Vol. 25, Feb. 1971, p. 69-72.

S. Yamamoto, et al., ''Coupled Strip Transmission Line with Three Center Conductors'', IEEE Trans.. Vol. MTT-14, Oct. 1966, p. 446-461.

W.J. Getsinger, ''Coupled Rectangular Bars Between Parallel Plates'', IRE Trans. Vol. MTT_10, Jan. 1962. p. 65-72.

W.J. Getsinger, ''A Coupled Strip-Line Configuration Using Printed Circuit Construction that Allows Very Close Coupling,'' IRE Trans., Vol. MTT-9, Nov. 961, p. 535-544.

J.D. Horgan, ''Coupled Strip Transmission Lines with Rectangular Inner Conductors,'' IRE Trans., Vol. MTT-5, April 1957, p. 92-99.

J.L. Allen and M.F. Estes, ''Broadside Coupled Strips in a Layered Dielectric Medium'', IEEE Trans., Vol. MTT-20, Oct. 1972, p. 662-668; Correction, MTT-23, Sept. 1975, p. 779.

I.J. Bahl and P. Bhartia, ''The Design of Broadside-Coupled Stripline Circuits,'' IEEE Trans., Vol. MTT-29, Feb. 1981, p. 165-168.

A.G. D'Assuncao, et al, ''Inhomogeneous Broadside-Coupled Striplines'', 1981 MTT Symposium Digest, p. 218-220.

J. Singletary, Jr., ''Fringing Capacitance in Stripline Coupler Design'' IEEE Trans., Vol. MTT-14, Aug. 1966, p. 398: Correction, MTT-15, March 1967, p. 200.

V.K. Tripathi, ''Asymmetric Coupled Transmission Lines in an Inhomogeneous Medium'', IEEE Trans., Vol. MTT-23, Sept. 1975, p. 734-739.

I.J. Bahl and P. Bhattia, ''Characteristics of Inhomogeneous Broadside-Coupled Striplines'', IEEE Trans., Vol. MTT-28, June 1980, p. 529-535.

I.J. Bahl and P. Bhartia, ''The Design of Broadside-Coupled Stripline Circuits'', IEEE Trans., Vol. MTT-29, Feb. 1981, p. 165-168.

A. Feller, H.R. Kaupp, et al, ''Crosstalk and Reflections in High-Speed Digital Systems,'' Proceedings—Fall Joint Computer Conference 1965, p. 511–525.

J. DeFalco, ''Predicting Crosstalk in Digital Systems,'' Computer Design June 1977, p. 69–75.

Standard Improvement Form

IPC-D-317A

The purpose of this form is to provide the Technical Committee of IPC with input from the industry regarding usage of the subject standard.

Individuals or companies are invited to submit comments to IPC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:

IPC
2215 Sanders Road
Northbrook, IL 60062-6135
Fax 847 509.9798

1. I recommend changes to the following:

___ Requirement, paragraph number _____

___ Test Method number _____, paragraph number _____

The referenced paragraph number has proven to be:

___ Unclear ___ Too Rigid ___ In Error

___ Other _____

2. Recommendations for correction:

3. Other suggestions for document improvement:

Submitted by:

Name Telephone

Company

Address

City/State/Zip Date

ANSI/IPC-T-50 Terms and Definitions for Interconnecting and Packaging Electronic Circuits Definition Submission/Approval Sheet

THE INSTITUTE FOR

INTERCONNECTING

AND PACKAGING

ELECTRONIC CIRCUITS

The purpose of this form is to keep current with terms routinely used in the industry and their definitions. Individuals or companies are invited to comment. Please complete this form and return to:

IPC
2215 Sanders Road
Northbrook, IL 60062-6135
Fax: 847 509.9798

SUBMITTOR INFORMATION:

Name: _____

Company: _____

City: _____

State/Zip: _____

Telephone: _____

Date: _____

❑ This is a **NEW** term and definition being submitted.
❑ This is an **ADDITION** to an existing term and definition(s).
❑ This is a **CHANGE** to an existing definition.

Term	Definition

If space not adequate, use reverse side or attach additional sheet(s).

Artwork: ❑ Not Applicable ❑ Required ❑ To be supplied
❑ Included: Electronic File Name: _____

Document(s) to which this term applies: _____

_____

_____

Committees affected by this term: _____

_____

_____

Office Use

IPC Office	**Committee 2-30**
Date Received: _____	Date of Initial Review: _____
Comments Collated: _____	Comment Resolution: _____
Returned for Action: _____	Committee Action: ❑ Accepted ❑ Rejected
Revision Inclusion: _____	❑ Accept Modify

IEC Classification

Classification Code • Serial Number

Terms and Definition Committee Final Approval Authorization:
Committee 2-30 has approved the above term for release in the next revision.

Name: _____ Committee: IPC 2-30 Date: _____

Technical Questions

The IPC staff will research your technical question and attempt to find an appropriate specification interpretation or technical response. Please send your technical query to the technical department via:

tel 847/509-9700 fax 847/509-9798
http://www.ipc.org e-mail: answers@ipc.org

IPC Technical Forums

IPC technical forums are opportunities to network on the Internet. It's the best way to get the help you need today! Over 2,500 people are already taking advantage of the excellent peer networking available through e-mail forums provided by IPC. Members use them to get timely, relevant answers to their technical questions.

TechNet@ipc.org

TechNet forum is for discussion of technical help, comments or questions on IPC specifications, or other technical inquiries. IPC also uses TechNet to announce meetings, important technical issues, surveys, etc.

ChipNet@ipc.org

ChipNet forum is for discussion of flip chip and related chip scale semiconductor packaging technologies. It is cosponsored by the National Electronics Manufacturing Initiative (NEMI).

ComplianceNet@ipc.org

ComplianceNet forum covers environmental, safety and related regulations or issues.

DesignerCouncil@ipc.org

Designers Council forum covers information on upcoming IPC Designers Council activities as well as information, comment, and feedback on current design issues,local chapter meetings, new chapters forming, and other design topics.

Roadmap@ipc.org

The IPC Roadmap forum is the communication vehicle used by members of the Technical Working Groups (TWGs) who develop the IPC National Technology Roadmap for Electronic Interconnections.

IPCsm840@ipc.org

This peer networking forum is specific to solder mask qualification and use.

ADMINISTERING YOUR SUBSCRIPTION STATUS:

All commands (such as subscribe and signoff) must be sent to listserv@ipc.org. Please DO NOT send any command to the mail list address, (i.e.<mail list> @ipc.org), as it would be distributed to all the subscribers.

Example for subscribing:
To: LISTSERV@IPC.ORG
Subject:
Message: subscribe TechNet Joseph H. Smith

Example for signing off:
To: LISTSERV@IPC.ORG
Subject:
Message: sign off DesignerCouncil

Please note you must send messages to the mail list address ONLY from the e-mail address to which you want to apply changes. In other words,if you want to sign off the mail list, you must send the signoff command from the address that you want removed from the mail list. Many participants find it helpful to signoff a list when travelling or on vacation and to resubscribe when back in the office.

How to post to a forum:

To send a message to all the people currently subscribed to the list, just send to <mail list>@ipc.org Please note, use the mail list address that you want to reach in place of the <mail list> string in the above instructions.

Example:
To: TechNet@IPC.ORG
Subject: <your subject>
Message: <your message>

The associated e-mail message text will be distributed to everyone on the list, including the sender. Further information on how to access previous messages sent to the forums will be provided upon subscribing.

For more information, contact Dmitriy Sklyar
tel 847/509-9700 x311 fax 847/509-9798
e-mail: sklydm@ipc.org http://www.ipc.org/html/forum.htm

IPC World Wide Web Page http://www.ipc.org

Our home page provides access to information about upcoming events, publications and videos, membership, and industry activities and services. Visit soon and often.

Education and Training

IPC conducts local educational workshops and national conferences to help you better understand emerging technologies. National conferences have covered Ball Grid Array and Flip Chip/Chip Scale Packaging. Some workshop topics include:

- Printed Wiring Board Fundamentals
- Troubleshooting the PWB Manufacturing Process
- Choosing the Right Base Material Laminate
- Acceptability of Printed Boards
- New Design Standards
- High Speed Design
- Design for Manufacturability
- Design for Assembly
- Designers Certification Preparation

IPC video tapes and CD-ROMs can increase your industry know-how and on the job effectiveness.

For more information on programs, contact John Riley
tel 847/509-9700 ext. 308 fax 847/509-9798
e-mail: rilejo@ipc.org http://www.ipc.org

For more information on IPC Video/CD Training, contact Mark Pritchard
tel 505/758-7937 ext. 202 fax 505/758-7938
e-mail: markp@taos.newmex.com
http://www.ipc.org

Training and Certification

IPC-A-610 Training and Certification Program

"The Acceptability of Electronic Assemblies" (ANSI/IPC-A-610) is the most widely used specification for the PWB assembly industry. An industry consensus Training and Certification program based on the IPC-A-610 is available to your company.

For more information, contact John Riley
tel 847/509-9700 ext. 308 fax 847/509-9798
e-mail: rilejo@ipc.org http://www.ipc.org/html/610.htm

IPC Printed Circuits Expo

IPC Printed Circuits Expo is the largest trade exhibition in North America devoted to the PWB industry. Over 90 technical presentations make up this superior technical conference.

IPC PRINTED CIRCUITS EXPO '98 — *April 28-30, 1998, Long Beach, California*

IPC PRINTED CIRCUITS EXPO '99 — *March 16-18, 1999, Long Beach, California*

For more information, contact Kim Behr
tel 847/509-9700 ext. 319 fax 847/509-9798
e-mail: behrki@ipc.org http://www.ipc.org

How to Get Involved

The first step is to join IPC. An application for membership can be found on page 74.
Once you become a member, the opportunities to enhance your competitiveness are vast. Join a technical committee and
learn from our industry's best while you help develop the standards for our industry. Participate in market research programs which forecast the future of our industry. Participate in Capitol Hill Day and lobby your Congressmen and Senators for better industry support. Pick from a wide variety of educational opportunities: workshops, tutorials, and conferences. More up-to-date details on IPC opportunities can be found on our web page: http:/www.ipc.org.

For information on how to get involved, contact:
Jeanette Ferdman, Membership Manager
tel 847/509-9700 ext. 309 fax 847/509-9798
e-mail: JeanetteFerdman@ipc.org http://www.ipc.org

APPLICATION FOR SITE MEMBERSHIP

Thank you for your decision to join IPC members on the "Intelligent Path to Competitiveness"! IPC Membership is **site specific,** which means that IPC member benefits are available to all individuals employed at the site designated on the other side of this application.

To help IPC serve your member site in the most efficient manner possible, please tell us what your facility does by choosing the most appropriate member category.

PLEASE CHECK APPROPRIATE CATEGORY

☐ INDEPENDENT PRINTED BOARD MANUFACTURERS

Our facility manufactures and sells to other companies, printed wiring boards or other electronic interconnection products on the merchant market.

WHAT PRODUCTS DO YOU MAKE FOR SALE?

- ☐ One-sided and two-sided rigid printed boards
- ☐ Multilayer printed boards
- ☐ Flexible printed boards
- ☐ Flat cable
- ☐ Hybrid circuits
- ☐ Discrete wiring devices
- ☐ Other interconnections

Name of Chief Executive Officer/President_____

☐ INDEPENDENT PRINTED BOARD ASSEMBLERS EMSI COMPANIES

Our facility assembles printed wiring boards on a contract basis and/or offers other electronic interconnection products for sale.

- ☐ Turnkey
- ☐ SMT
- ☐ Chip Scale Technology
- ☐ Through-hole
- ☐ Mixed Technology
- ☐ Consignment
- ☐ BGA

Name of Chief Executive Officer/President_____

☐ OEM – MANUFACTURERS OF ANY END PRODUCT USING PCB/PCAS OR CAPTIVE MANUFACTURERS OF PCBS/PCAS

Our facility purchases, uses and/or manufactures printed wiring boards or other electronic interconnection products for our own use in a final product. Also known as original equipment manufacturers (OEM).

IS YOUR INTEREST IN:

- ☐ purchasing/manufacture of printed circuit boards
- ☐ purchasing/manufacturing printed circuit assemblies

What is your company's main product line? _____

☐ INDUSTRY SUPPLIERS

Our facility supplies raw materials, machinery, equipment or services used in the manufacture or assembly of electronic interconnection products.

What products do you supply?_____

☐ GOVERNMENT AGENCIES/ ACADEMIC TECHNICAL LIAISONS

We are representatives of a government agency, university, college, technical institute who are directly concerned with design, research, and utilization of electronic interconnection devices. (Must be a non-profit or not-for-profit organization.)

Please be sure both sides of this application are correctly completed

APPLICATION FOR SITE MEMBERSHIP

Site Information:

Company Name

Street Address

City | State | Zip | Country

Main Phone No. | Fax

Primary Contact Name

Title | Mail Stop

Phone | Fax | e-mail

Alternate Contact Name

Title | Mail Stop

Phone | Fax | e-mail

Please check one:

❑ $1,000.00 Annual dues for Primary Site Membership (Twelve months of IPC membership begins from the time the application and payment are received)

❑ $800.00 Annual dues for Additional Facility Membership: Additional membership for a site within an organization where another site is considered to be the primary IPC member.

❑ $600.00** Annual dues for an independent PCB/PWA fabricator or independent EMSI provider with annual sales of less than $1,000,000.00. **Please provide proof of annual sales.

❑ $250.00 Annual dues for Government Agency/University/not-for-profit organization

TMRC Membership ❑ Please send me information on Membership in the Technology Marketing Research Council (TMRC)

AMRC Membership ❑ Please send me information for Membership in the Assembly Marketing Research Council (AMRC)

Payment Information

Enclosed is our check for $_____

Please bill my credit card: (circle one) MC AMEX VISA DINERS

Card No. _____ Exp date _____

Authorized Signature _____

Mail application with check or money order to:

IPC
Dept. 77-3491
Chicago, IL 60678-3491

Fax/Mail application with credit card payment to:

IPC
2215 Sanders Road
Northbrook, IL 60062-6135
Tel: 847 509.9700
Fax: 847 509.9798

PLEASE ATTACH BUSINESS CARD OF OFFICIAL REPRESENTATIVE HERE

2215 Sanders Road
Northbrook, Illinois
60062-6135

Tel 847 509.9700
Fax 847 509.9798
URL: http://www.ipc.org